

Downloading to XC3S100E

PURPOSE -- This lab will present a brief overview of the XC3S100E FPGA Board (of Digilent) and how to download bitstream (the result of the implementation of a design) files to it.

1. Introduction to the XC3S100E FPGA and BASYS Board.

In this lab you will become familiar with BASYS FPGA Board (of Digilent) to which you will download your bitstream created during the lab #1. You may want to read the board description manual now, which can be found as a pdf document on the web page of your class.

The BASYS board provides an ideal circuit design platform for anyone who wants to learn about FPGAs and digital circuit design. It combines the advanced features of Xilinx's Spartan-3E FPGA with straightforward power supply and I/O circuits, making it the perfect platform for introductory designs ranging from simple logic circuits to complex digital systems.

The four on-board 6-pin connectors can accommodate any of Digilent's low-cost "PMOD" accessory circuits, making it easy to add A/D and D/A converters, motors, sensors, and a variety of other devices and circuits.

The BASYS board is fully compatible with all versions of the Xilinx ISE tools, including the free WebPack.

Features:

- 100K- gate Xilinx Spartan 3-E FPGA that features four 18-bit multipliers, 72Kbits of fast dual-port block RAM and 500MHz+ operation
- JTAG programming port (programming cable included)
- XCF02 Platform Flash ROM that stores FPGA configurations indefinitely
- User-settable oscillator frequency (25, 50, and 100 MHz), plus socket for a second oscillator
- Three on-board voltage regulators (1.2V, 2.5V, and 3.3V) that allow use of 4V-12V external supplies (power supply included)
- 8 LEDs, 4-digit seven-segment display, four pushbuttons, 8 slid switches, PS/2 port, and a 3-bit VGA port
- Four 6-pin headers for user I/Os, and attaching Digilent PMOD accessory circuit boards

NOTE: Take a few minutes and read the manual of the XC3S100E FPGA. It can be found as a pdf document on the web page of your class.

NOTE: Note that the bitstream that you download to the FPGA is volatile, which means that the FPGA is erased every time the power is removed. The BASYS board can be reprogrammed an unlimited number of times. If you need the FPGA board to retain its bitstream even when power is removed you need to download the bitstream to the Flash and make it "permanent," but you will not be doing this in this class.

After a bitstream has been downloaded to the BASYS board, you need some way to test the design. *You will be using the 8 DIP switches (slid switches) of the BASYS board as inputs a[0-3] and b[0-3] and a pushbutton as input ci for your adder. To better understand the way you will excite the inputs of your adder, use the manual of the BASYS board to see how the outputs of your adder are directed to 5 (five) bargraph LEDs of the BASYS board! A fully understanding of these pin assignments and how they work is obligatory, to understand the way you will verify your designs later.*

2. Downloading to the BASYS Board

After you performed Implementation during the previous laboratory, and looked inside your project directory, you saw a file called fourbit_adder.bit under the directory of your project. This is the file that will be downloaded to the BASYS board.

Before you download to the BASYS board, make sure that the parallel port connector is properly connected to the BASYS board. Also make sure that the power supply is plugged into the BASYS board. When it's plugged in, the 7 segment LED display on the board should be lit. If it is not lit at all, then something may be wrong.

Open your previous project (lab02). Please verify that you have implemented the design (or Rerun Implement Design) without any errors. Now, click on the '+' sign next to the "Generate Programming File" menu.

Now double click "**Configure Device (iMPACT)**". A new window (iMPACT) will pop up. Please select "**Configure devices using Boundary-Scan (JTAG)**" with default option (Automatically connect to a cable and identify Boundary-Scan chain) as the action from the list. A progress dialog will appear. Once the identification process is complete another small window "Assign a New Configuration File" will appear. Please select **fourbit_adder.bit** (or other *.bit, if you have named your project top-module file differently). Here you are assigning the file/ program that has be to be programmed into the **XC3S100E FPGA**. Once again the same window will appear. This time it is asking for the file/ program to be programmed into the **XCF02 Platform Flash ROM**. Please select "**BYPASS**". If you assign any file to this ROM, the default program & FPGA configuration will be erased (And if the program has any errors, the board will become useless and will have to replaced)

Now right click on **XC3S100E FPGA** block and select "Program". To accept the default values in the "Programming Properties", click OK. If all the connections are correct a progress dialog will appear and "Programming Succeeded" message will flash.

Once the files have been downloaded you may remove the JTAG programming cable connection from the board. Some of the parallel port pins also drive BASYS board devices like the 7 segment LEDs and will cause interference with the operation of the BASYS board.

NOTE: Unplugging the power supply from the BASYS board will erase the bitstream in the FPGA. You must re-download the bitstream each time power is removed.

3. Verifying the design

Once you have loaded the BASYS Board with a configuration file using iMPACT, you can start verifying your adder. Use the assigned DIP switches to excite a and b input vectors and the pushbutton to excite the carry-in of your adder. Watch the corresponding bargraph LEDs (i.e. the output **y** and the **carry-out** of your adder) to see the correctness of your adder.

Take a few minutes and play with it. Try to understand completely every aspect of this verifying step.

SUMMARY -- This lab was about downloading a bitstream to an FPGA mounted on the BASYS board. You should now be familiar with BASYS board and how it work.
