

## Lab Report Guidelines

- The lab report will be on the FPGA design flow practiced in labs one to four.
- The intent of this report is not to rewrite the procedures practiced in lab, but to focus on the different steps of the design flow, namely design entry, synthesis, implementation, and bit generation and downloading on to the FPGA.
- It is highly recommended that you read the help files inside Xilinx ISE.
- Here is the report format:
  - Overall length 3-4 pages
  - Content
    - Introduction
      - Brief discussion of how FPGA design is useful.
      - Brief discussion of the overall design flow (with block diagram illustration) and how design verification fits in this overall picture.
      - Brief discussion of how the Xilinx tools in lab can be used to perform the design flow.
    - Body
      - One section for each major step of the design flow
        1. Discuss what is performed during the step
        2. Explain what are the input files of the step
        3. Explain what output files are produced by the step
      - One section for each lab (1-4)
        1. Discuss what we did in the lab
          - Steps (What you did/created/simulated etc)
          - Outcome (What you accomplished/learned)
        2. Illustrate how this lab fits into the overall design flow
    - Summary
      - Put it all together: Summarize design flow and how our labs fit in.

Note: You will be graded on content and presentation.