1. A 4-word direct-mapped cache uses a block size of 1 word. The current contents of the cache are as follows (note: the tag and data entries are specified in hex):

<table>
<thead>
<tr>
<th>block</th>
<th>valid</th>
<th>tag</th>
<th>data</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>0004000</td>
<td>00000000</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>000A000</td>
<td>11111111</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0001000</td>
<td>22222222</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>0006000</td>
<td>33333333</td>
</tr>
</tbody>
</table>

The contents of memory starting at hex address 00010000 are the following bytes, specified in hex: 00, 11, 22, 33, 44, 55, 66, 77, 88, 99, AA, BB, CC, DD, EE, FF.

A 32-bit MIPS processor generates the following sequence of addresses: 00040000, 00010008, 0001000C, 00010004, 00010008, 0001000C, 00010000.

(a) (14 points) For each of these addresses, indicate whether a hit or a miss occurs. State the reasons why each one is a hit or a miss.

(b) (20 points) Give the final contents of the cache (showing all of the entries in the block, valid, tag and data columns) after this series of addresses has been processed.

2. Consider the following portion of a VeSPA assembly language program:

```
add r4, r5, r6 ; instruction 1
sub r6, r7, r5 ; instruction 2
or  r4, r6, r4 ; instruction 3
```

(a) (16 points) Identify any flow dependences, anti-dependences and output dependences that exist amongst these instructions. (In each case, specify the register that is involved.)

(b) (16 points) Suppose that instruction 1 is in the instruction fetch (IF) stage of the 5-stage pipelined VeSPA implementation during cycle 11. Determine which cycles instructions 1, 2 and 3 will be in the write back (WB) stage of the pipeline. (Include a table that shows the instructions moving through the pipeline as part of your answer.)

3. On a certain processor the multiply instruction takes 15 cycles and accounts for 20% of the instructions in a typical program, while the other 80% of the instructions require an average of 5 cycles for each instruction.

(a) (14 points) What percentage of the time does the CPU spend doing multiplication?

(b) (20 points) A proposed design change will reduce the number of cycles required for a multiply instruction to 10, but the cycle time of the processor would have to be increased by a factor of (7/5). Would this design change improve the overall performance of the processor? Explain your answer.