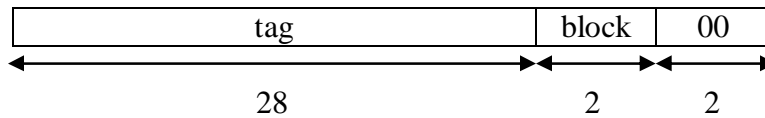


EE 4363 /CSci 4203 – Spring, 2006 – Midterm Exam 2 Solutions

1. (a) The direct-mapped cache has 4 blocks, with one word per block. Therefore, an address is partitioned into the following fields:



Thus, the tag consists of the 7 high-order hex digits of the address, while the block field is the 2 most-significant bits of the lowest-order hex digit.

The hits/misses are as follows:

- 00040000: block = 0 => hit (because valid = 1 and tag matches)
- 00010008: block = 2 => miss (because valid = 0);
data updated to 8899AABB and valid bit set to 1
- 0001000C: block = 3 => miss (because valid = 0 and tag does not match);
tag updated to 0001000, data updated to CCDDEEFF and valid set to 1
- 00010004: block = 1 => miss (because tag does not match);
tag updated to 0001000, data updated to 44556677
- 00010008: block = 2 => hit (because valid = 1 and tag matches)
- 0001000C: block = 3 => hit (because valid = 1 and tag matches)
- 00010000: block = 0 => miss (because tag does not match);
tag updated to 0001000, data updated to 00112233

Thus, the final cache contents will be:

block	valid	tag	data
0	1	0001000	00112233
1	1	0001000	44556677
2	1	0001000	8899AABB
3	1	0001000	CCDDEEFF

2.

```

add r4, r5, r6 ; instruction 1
sub r6, r7, r5 ; instruction 2
or r4, r6, r4 ; instruction 3
    
```

(a) flow dependence from instruction 1 to instruction 3 through r4

flow dependence from instruction 2 to instruction 3 through r6

instruction 1 is anti-dependent on instruction 2 through r6

instructions 1 and 3 are output dependent through r4

(b)

	IF	ID	EX	MEM	WB
11	add				
12	sub	add			
13	or	sub	add		
14		or	sub	add	
15			or	sub	add
16				or	sub
17					or

(no bubbles are inserted because of the forwarding logic in the pipelined VeSPA implementation). Thus:

instruction 1 will be in the WB stage during cycle 15
instruction 2 will be in the WB stage during cycle 16
instruction 3 will be in the WB stage during cycle 17

3. (a) The average CPI is: $(0.2)(15 \text{ cycles/instruction}) + (0.8)(5 \text{ cycles/instruction}) = 3 + 4 \text{ cycles/instruction} = 7 \text{ cycles/instruction}$. Of that, $(0.2)(15 \text{ cycles/instruction}) = 3 \text{ cycles/instruction}$ are due to multiplications. Thus, multiplications take up $3/7$, or approximately 43% of the CPU time.

(b) After making the proposed change, the average CPI would be: $(0.2)(10 \text{ cycles/instruction}) + (0.8)(5 \text{ cycles/instruction}) = 2 + 4 \text{ cycles/instruction} = 6 \text{ cycles/instruction}$. However, the clock rate is increased by a factor of $(7/5)$. So, the new performance will be $(7/6)(5/7) = 5/6$ times as good as the original design. Therefore, the modification would reduce the performance and it should not be made.