EE 4363 /CSci 4203 – Spring, 2007 – Midterm Exam 2 Solutions

1.

```
add  r7, r8, r9     ;    instruction 1
sub  r9, r1, r8     ;    instruction 2
or   r7, r9, r1     ;    instruction 3
```

(a) flow dependence from instruction 2 to instruction 3 through r9

instruction 1 is anti-dependent on instruction 2 through r9

instructions 1 and 3 are output dependent through r7

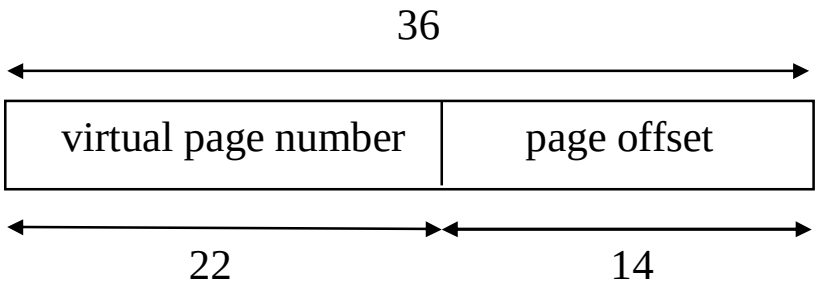
(b)

	IF	ID	EX	MEM	WB
21	add				
22	sub	add			
23	or	sub	add		
24		or	sub	add	
25			or	sub	add
26				or	sub
27					or

(no bubbles are inserted because of the forwarding logic in the pipelined VeSPA implementation). Thus:

instruction 1 will be in the WB stage during cycle 25
instruction 2 will be in the WB stage during cycle 26
instruction 3 will be in the WB stage during cycle 27

2. page size of 16K bytes => 14-bit page offset => 36 – 14 = 22-bit virtual page number:



=> number of page table entries is 2^{22}

each entry is 32 bits = 4 bytes

=> total size of the page table = $(2^{22})(2^2$ bytes) = 2^{14} Kbytes

3. hits and misses are as follows:

6-miss, 7-miss, 14-miss, 12-miss, 6-hit, 22-miss, 23-miss, 15-miss, 4-miss, 7-miss, 22-hit, 20-miss, 4-hit, 6-hit

The final cache contents are as follows:

set	address
0	
1	
2	
3	
4	~~12~~ 20 4
5	
6	6 ~~14~~ 22
7	~~7~~ 15 ~~23~~ 7

4.

(a) The average CPI = (0.2)(20) + (0.8)(5) = 4 + 4 = 8 cycles per instruction. The multiply instructions use (0.2)(20) = 4 cycles per instruction of that, so the CPU spends 4/8 = 0.5 = 50% of the time doing multiplication.

(b) After the change, the average CPI = (0.2)(10) + (0.8)(5) = 2 + 4 = 6 cycles per instruction but the clock cycle time is 5/4 as long as before. So, after the change, the machine will be faster by a factor of (8/6)(4/5) = 32/30 = 16/15. So, “it would be 16/15 times faster.”