1. Consider the following portion of a VeSPA assembly language program:

\[
\begin{align*}
&\text{xor } r7, r8, r9 \quad ; \quad \text{instruction 1} \\
&\text{add } r9, r1, r8 \quad ; \quad \text{instruction 2} \\
&\text{sub } r4, r9, r1 \quad ; \quad \text{instruction 3} \\
&\text{add } r3, r9, r2 \quad ; \quad \text{instruction 4} \\
&\text{and } r7, r2, r3 \quad ; \quad \text{instruction 5} \\
&\text{or } r8, r7, r4 \quad ; \quad \text{instruction 6}
\end{align*}
\]

(a) (12 points) Identify the flow dependences that exist amongst these instructions. In each case, specify the register that is involved.

(b) (13 points) Suppose that instruction 1 is in the instruction fetch (IF) stage of the 5-stage pipelined VeSPA implementation during cycle 11. Determine which registers are being read from and written to the register file during cycle 16. Include a very brief explanation of your answer.

2. (20 points) Consider the following parameter values: memory is byte-addressable, the virtual address is 34 bits, the page size is 64K bytes and each page table entry is 24 bits. Determine the number of bits in the virtual page number field, the number of bits in the page offset field, the number of page table entries and the total size (in Kbytes) of the page table.

3. (30 points) Here is a series of address references given as word addresses: 1, 17, 13, 1, 6, 22, 21, 5, 14, 6, 5, 1, 21, 17, 1, 5, 6, 22. Show the hits and misses and the final cache contents for a 4-way set-associative cache with one-word blocks and a total size of 16 words. Assume that LRU replacement is used.

4. Two programs, P1 and P2, are executed on two different computers, C1 and C2. On C1, P1 takes 6 seconds and P2 takes 12 seconds. On C2, P1 takes 4 seconds and P2 takes 16 seconds. For P1, \(4 \times 10^9\) instructions are executed on C1 and \(5 \times 10^9\) instructions are executed on C2. C1 has a clock rate of 2 GHz and C2 has a clock rate of 5 GHz.

(a) (12 points) Find the clock cycles per instruction (CPI) for P1 on C1 and C2.

(b) (13 points) Suppose that the CPI for P2 on C1 is the same as the CPI for P1 on C1 and that the CPI for P2 on C2 is the same as the CPI for P1 on C2. Determine the number of instructions executed for P2 on C1 and C2.