Spring 2006 EE 5327 VCS Quick Tutorial

SETUP:

1. Use a text editor to put those settings in your ".cshrc" file.

```
# for vcs
setenv SNPSLMD_LICENSE_FILE 27000@dogbert.itlabs.umn.edu
setenv VCS_HOME /synopsys/vcs
set path=(/synopsys/vcs/bin /usr/ccs/bin $path)
```

2. Save ".cshrc" file and quit the text editor.
3. Source ".cshrc" file by typing the following command at UNIX command prompt. (Note that you DON'T have to do this in your next login and beyond.)

```
source .cshrc
```

Download example source codes:

4. There are four source codes. Download them to your account.

```
ripple.v      fulladd.v     fulladd1.v      fulladd2.v
```

Compilation and Simulation with VirSim:

5. Use the following command to do compilation and invoke VirSim. After you enter this command, you'll see the VirSim compiler window being popped up and in your working directory there'll be an executable file `simv` and two folders (`csrc/` and `sim.daidir/`) that contain the object files and libraries that VCS uses to create the executable file.

```
vcs -Mupdate -RI ripple.v
```

Where:

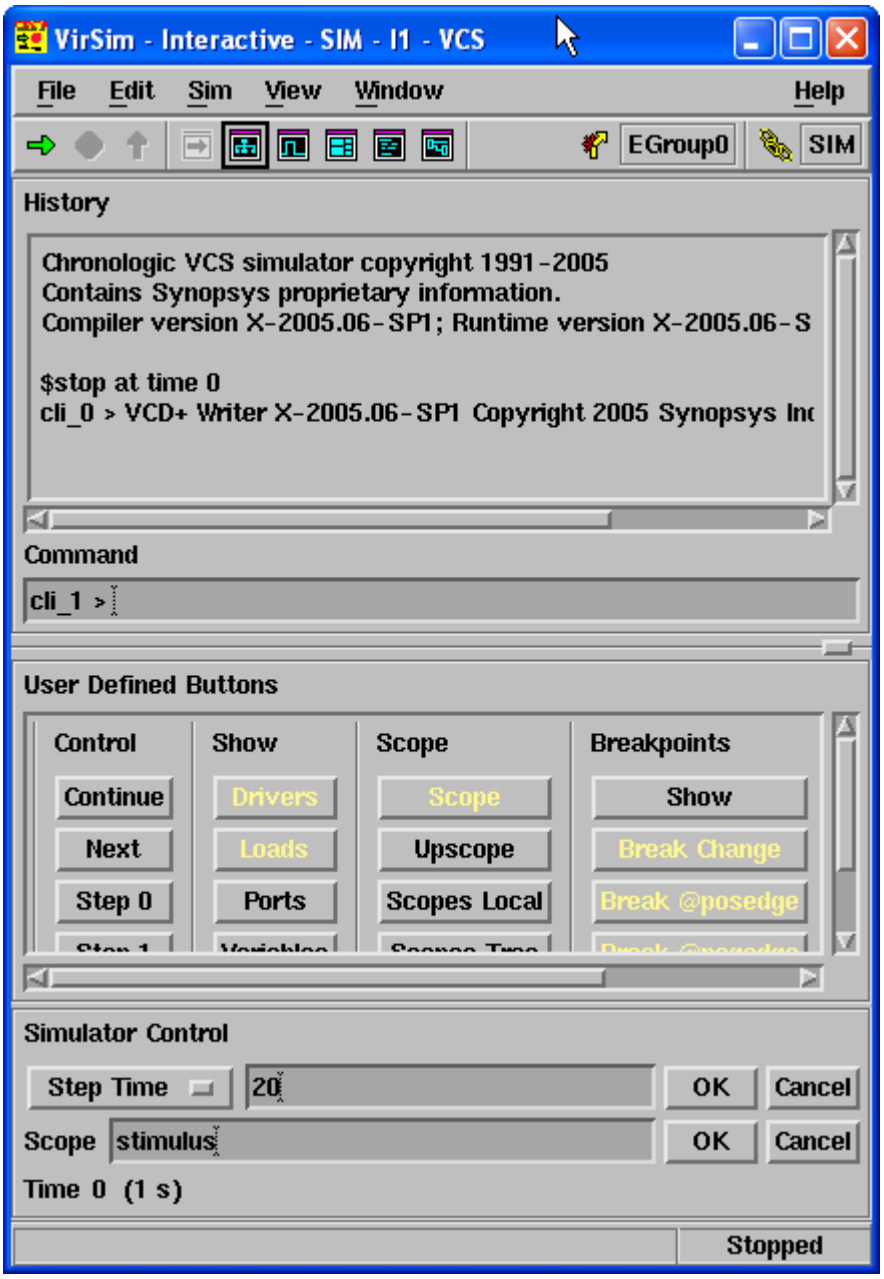
vcs Is the command that starts the Verilog compiler.

-Mupdate Is a compile-time option. Compile-time options control how VCS compiles your source code. There are also run-time options that control how VCS simulates your design. This compile-time option specifies incremental compilation and update the makefile. Incremental compilation is compiling only the modules that have changed since you last compiled the source file. Using this compile-time option now, even though you have never compiled any of the design's modules before is worthwhile because this option also tells VCS to create a subdirectory in your current directory named csrc and in that subdirectory are object files, and in some cases C or assembly intermediate files, and files that VCS uses to determine if it needs to compile a module over again. The makefile contains commands that VCS uses to generate object files, sometimes C or assembly files, and build the executable that you simulate. Over-writing the makefile with a new one ensures that VCS does not

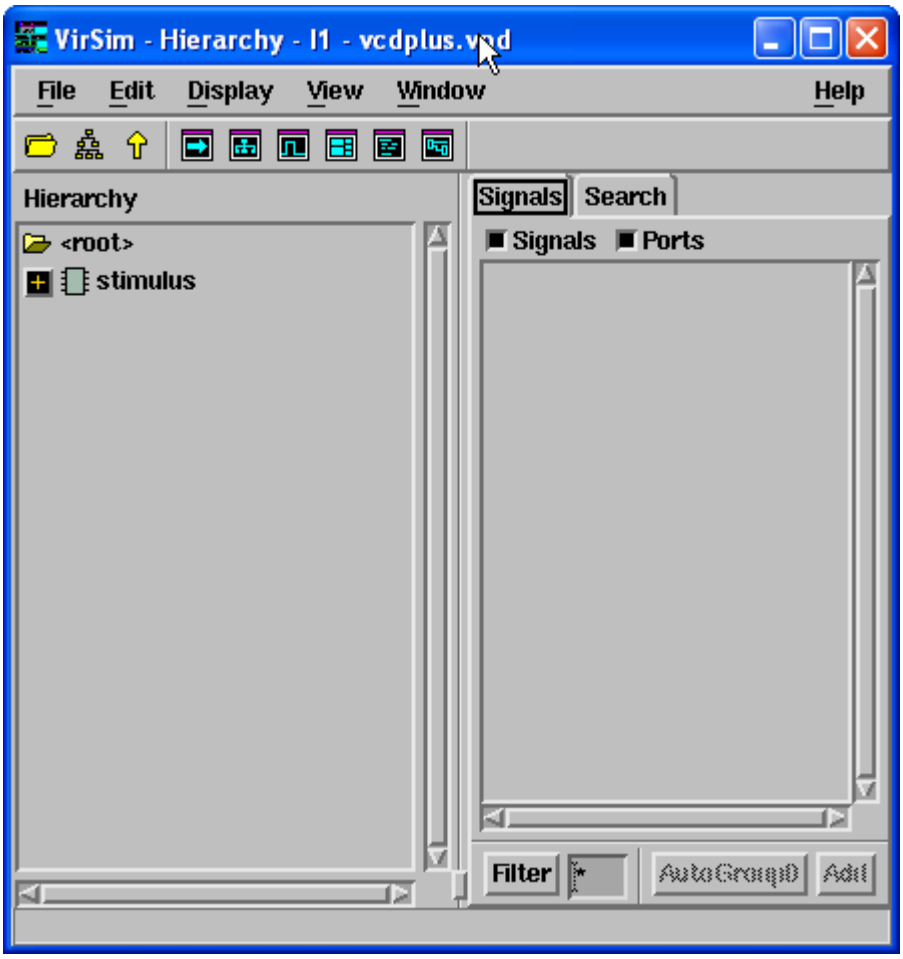
use a makefile that is out of date for your design. We recommend that you always use the -Mupdate compile-time option.

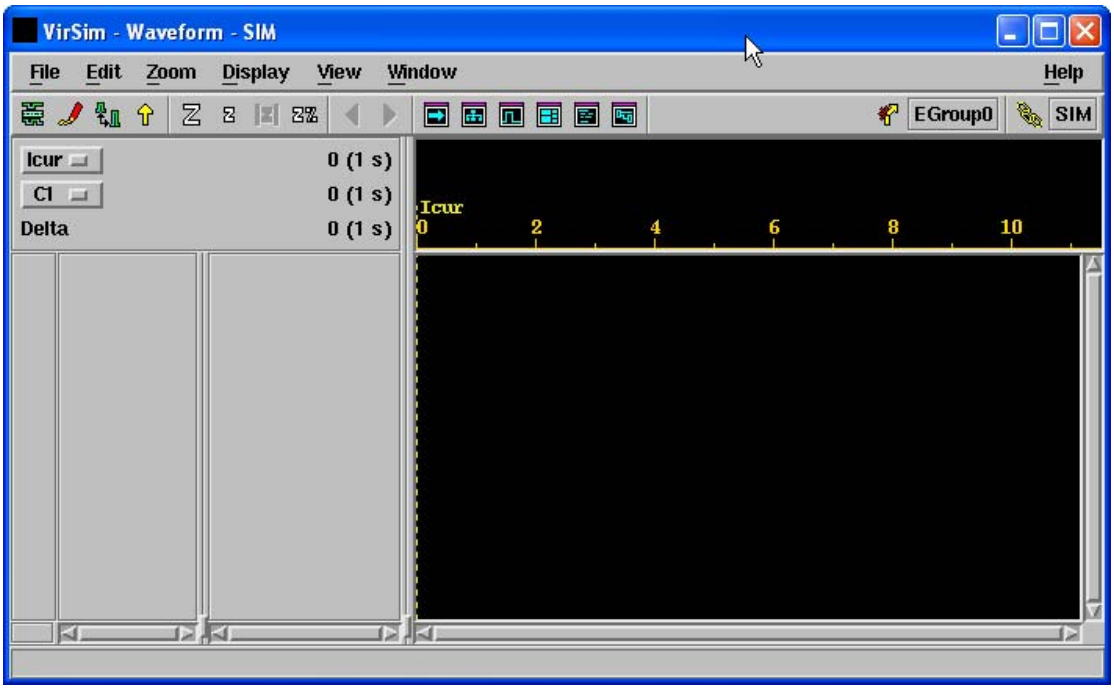
-RI This compile-time option tells VCS to start simulation immediately after compilation and start VirSim. Think of this option as telling VCS to Run Interactively after it compiles your source code.

6. The popped up window is VirSim Interactive window that looks like this.



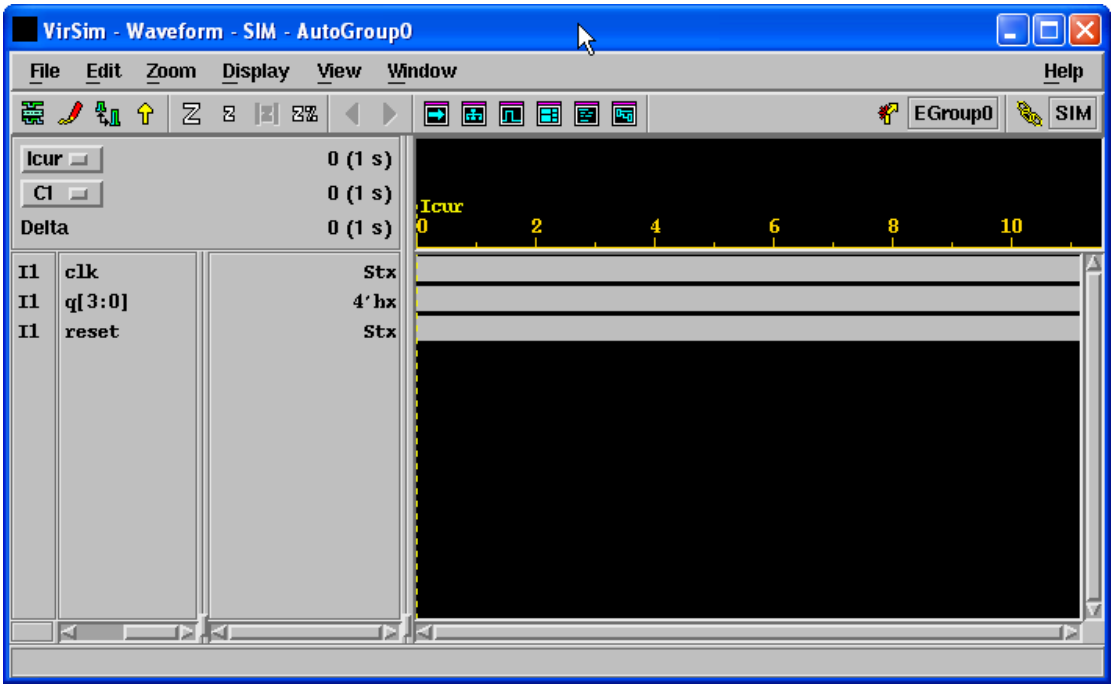
7. Click on `Window/Hierarchy` and `Window/Waveform` respectively to bring up the hierarchy and waveform windows. They look like those below.



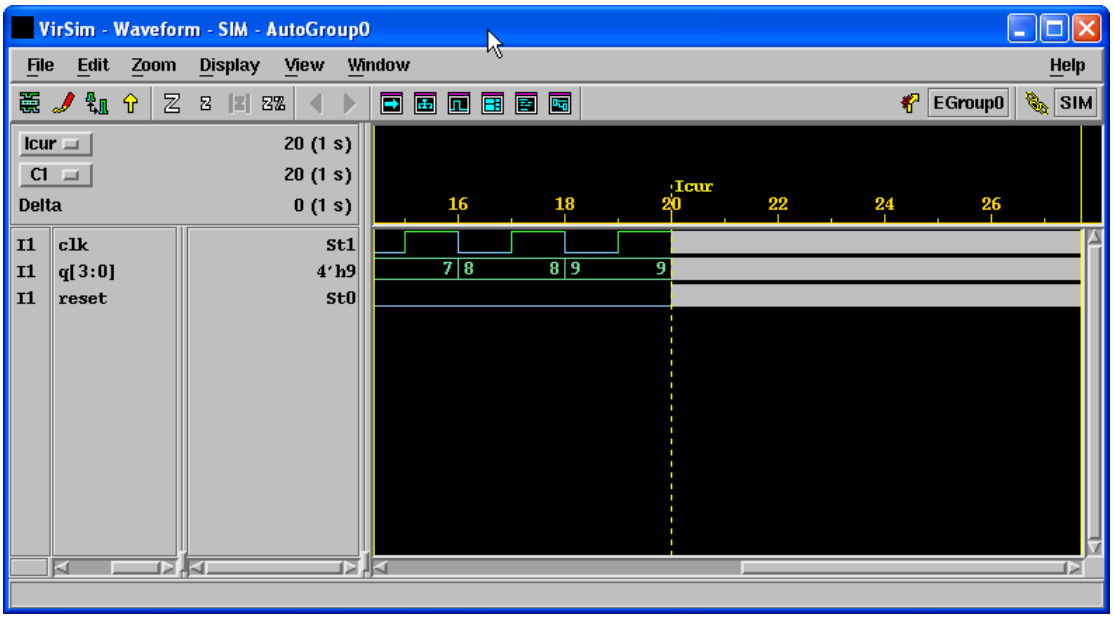


8. Click on `stimulus` in the Hierarchy window and then the signals will be listed on the right-hand side pane.
9. Select all the signals and drag them (using middle button of your mouse) into

the waveform window.



10. In the interactive window, there are three panes. The bottom pane is `Simulator Control` where you click on the upper `OK` button that will trigger the simulator to run 20 sec. The waveform window will look like this.



11. You may click on  to zoom to 100% in order to see the whole 20 sec waveform.
12. Repeat on the other three four-bit adder examples.

Credit: Some points have been borrowed from Synopsys VCS and VirSim Tutorial.