SIMULTANEOUS BI-DIRECTIONAL SIGNALING WITH ADAPTIVE PRE-EMPHASIS

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ABSTRACT

This paper presents a novel design for a simultaneous bi-directional signaling system with an adaptive pre-emphasis feature. The feedback loop inherent in a simultaneous bi-directional link provides a natural opportunity to use adaptive pre-emphasis to compensate for channel characteristics. The system determines the degree of corruption of a received signal and generates a pulse width modulated signal which gets sent back through the bi-directional link to control the amount of pre-emphasis that is used. The technique has been verified using Cadence SpectreRF and Verilog-A simulators, where the channel loss characteristics are based on an FR-4 material model. The simulation results show that the system automatically selects the best fit for the observed channel loss compensation, which then reduces the efforts needed to recover the data at each receiver.

1. INTRODUCTION

Modern semiconductor technology allows for the design of integrated circuits operating with on-chip clock frequencies easily beyond a gigahertz. However, the overall performance of a system depends not only on the speed of on-chip computations but also the throughput of the I/O. Pin-count limits and maximum achievable I/O bandwidth have proven to be major challenges to overall system performance. The need for higher total I/O bandwidth has led several researchers to study simultaneous bi-directional signaling [1-5]. For a given total I/O bandwidth, simultaneous bi-directional signaling offers higher timing margin but lower voltage margin. Therefore, it is most suitable for use in low loss or short link communications [6].

Bi-directional signaling is attractive because of the capability of simultaneously sending and receiving data across the same channel. It doubles the effective throughput for a given pin-count compared to the traditional unidirectional signaling. The basic circuit diagram and an illustration of the input/output signals for simultaneous bi-directional signaling are shown in Figures 1 and 2, respectively. Replica-Diver.L and Replica-Driver.R have the same characteristics as Driver.L and Driver.R, respectively. Therefore, echo cancellation can completely remove its own side driver outgoing signal and extract the received signal, VIL(T_O) or VIR(T_O). (T_O represents the delay time for the wave traveling through the channel.) A 3-level signal is seen on the channel even though it is only a 2-level signal transmission system. The feedback loop inherent in the bi-directional link provides a natural opportunity for using an adaptive pre-emphasis design.

Our design approach is to first determine the degree of degradation on the received signal. Then, the sub-system generates a moderately low frequency (e.g. 1/10 the normal data rate) pulse width modulated signal which gets fed back to the transmitting side through the existing simultaneous bi-directional link. The moderately low frequency provides minimum signal loss on the transport channel. The pulse width modulated signal is then averaged and used to adjust the amplitude of pre-emphasis applied at the transmitter.

Prior work on pre-emphasis to compensate for channel characteristics has been done in the context of Fast Ethernet and high-speed cable links [7-9]. However, these systems require an extra dedicated wire to carry the control signal back to the transmitter. The novelty of our approach is that we make use of the inherent bi-directional nature of the link to carry the control information without any additional wire, as well as the fact that the pre-emphasis is applied to signals propagating in both directions.

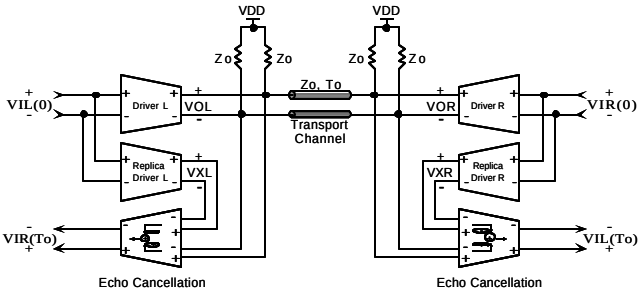

Figure 1. The basic circuit diagram for simultaneous bi-directional signaling.

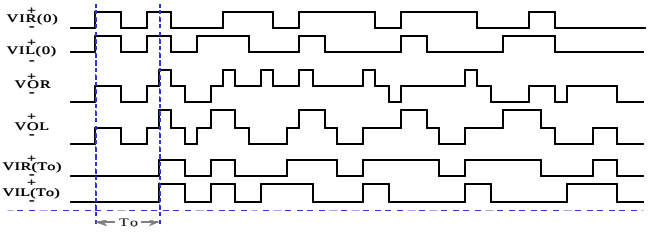

Figure 2. Input/output signals in a simultaneous bi-directional signaling system.

2. SYSTEM ARCHITECTURE

Simultaneous bi-directional signaling systems can be defined as either current-mode or voltage-mode and as differential or single-ended signaling systems. A current-mode driver draws constant current though the termination load and therefore consumes more power, but it has better impedance matching and smaller reflections than a voltage-mode driver. Furthermore, a current-mode driver potentially provides higher bandwidth than a voltage-mode driver because the equivalent load on the output of the driver is $Z_O / 2$ and $Z_O \times 2$ for current-mode and voltage-mode, respectively. For the same parasitic capacitance associated with a driver output load, a current-mode driver has 4 times as much bandwidth as a voltage-mode driver. The difference between differential and single-ended signaling is that the former is immune to common-mode noise (e.g. substrate noise) but has only half of the total I/O bandwidth compared to latter. Since a high-speed simultaneous bi-directional signaling system would be sensitive to impedance mismatch and noise, we have chosen to implement a configuration based on a differential current-mode driver for our study of adaptive pre-emphasis.

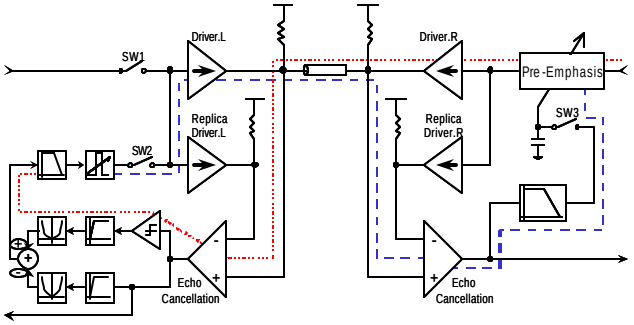

Figure 3. The proposed simultaneous bi-directional signaling system with adaptive pre-emphasis. (Only side of the pre-emphasis circuitry is shown.)

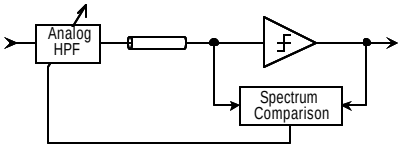

Figure 4. A conceptual circuit diagram for implementing adaptive pre-emphasis.

Figure 3 shows the basic circuit diagram for our proposed system. For simplicity and readability, the figure has been drawn in a single-ended mode. For comparison, Figure 4 shows the conceptual circuit diagram of an adaptive pre-emphasis scheme that was used in a tunable cable equalizer [7]. The dotted line in Figure 3 shows the normal high-speed data path from right to left through the transport channel. The signal is then divided into two paths after echo cancellation. The two paths include a comparator, two low-pass filters, two full-wave rectifiers and a subtraction representing the spectrum comparison block of Figure 4. The spectrum comparison design is based on the adaptive equalizer of Ref. [8]. The difference between the two paths is then averaged through a low-pass filter and is used to generate a pulse-width modulated signal at 1/10 the normal data rate. The low speed pulse-width modulated signal is then sent back to the right side of the system through the transport channel following the dashed line of Figure 3. The received pulse-width modulated signal is averaged through a low pass filter and is used to tune the amplitude of the pre-emphasis. Figure 5 shows an example circuit schematic for a current-mode logic (CML) transmitter driver with an adjustable 1-tap pre-emphasis. For our design, the transmitter driver pre-emphasis has been implemented with a constant current difference between driver and pre-emphasis paths so that the amplitude of the signal eye opening is always kept constant.

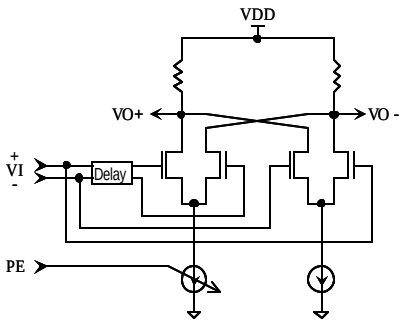

Figure 5. Example circuit schematic for a current-mode logic (CML) transmitter driver with an adjustable 1-tap pre-emphasis.

The design of the echo cancellation circuit is shown in Figure 6 which is also based on the adaptive equalizer of Ref. [8]. A detailed analysis of the adaptive equalizer is available in Ref. [9]. However, a high-pass filter is used instead of a low-pass filter before the variable gain amplifier. The justification for this is that Driver.L and Driver.R always drive I/O and the off-chip transport channel and are always more bandwidth limited than Replica-Driver.L and Replica-Driver.R of Figure 1. The circled dashed line area represents the tunable low-pass filter.

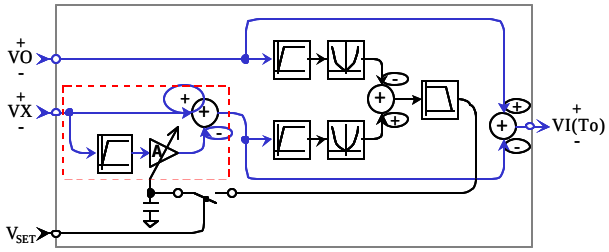

Figure 6. The basic circuit diagram of echo cancellation.

The proposed simultaneous bi-directional signaling system uses the following operational sequence:

a. Run an echo cancellation initialization setup individually with the channel and all interconnects presented and the opposite side driver turned off.

b. Run an adaptive pre-emphasis initialization setup with the channel and all interconnects presented. SW1, SW2 and SW3 in Figure 3 are "OFF", "ON" and "ON" respectively.

c. Normal simultaneous bi-directional signaling can proceed after steps a. and b. If the channel or interconnects are modified, steps a. and b. have to be revisited before continuing the bi-directional signaling.

The system can also be set up so that it will automatically revisit steps a. and b. after certain time periods in order to ensure that the echo cancellation and the adaptive pre-emphasis are still operating correctly.

3. SIMULATION RESULTS

The proposed design has been verified using Cadence SpectreRF and Verilog-A simulations. The channel loss characteristic is based on a model of FR-4 material which is the standard glass epoxy substrate having approximately 1 dB loss per inch at 10 GHz [10]. Figure 7.(1) shows simulation results for the signal loss in the channel versus signal frequency at 2", 4", 6", 8" and 10" lengths. Figure 7.(2) – (4) show the simultaneous bi-directional signaling transient simulation results at 5 Gbps for the circuit of Figure 1. Input and output signal eye-diagrams of the driver show the 3-level characteristic on the transport channel even though it is still a 2-level data transmission system. The transport channel length used for the transient simulation in Figure 7 is 10 inches long and the driver input signals, VIR(0) and VIL(0), are different pseudo-random binary sequences (PRBSs) at $2^7 - 1$ bits.

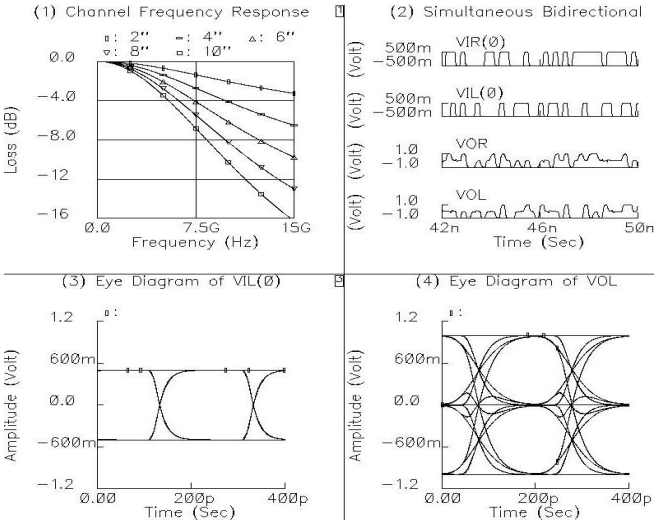

Figure 7. The simultaneous bi-directional signaling simulation results for the circuit of Figure 1.

Figure 8 shows the echo cancellation initialization setup simulation results for the circuits of Figures 1 and 6. The damping factor is set to be close to 0.707 for the tunable low-pass filter used in the echo cancellation so that the initialization time is optimized without stability concerns. The required initialization time is less than 2 uS after reaching the steady-state mode and is shown in Figure 8.(1). The output of the echo cancellation shown in Figure 8.(2) and (4) should as small as possible in order to minimize the degradation of the received signal.

Figure 9 shows the adaptive pre-emphasis initialization setup simulation results for the circuit of Figure 3. The required initialization time is also less than 2 uS after reaching the steady-state mode, as shown in Figure 9.(1) and (2). The transient signal amplitude at the data driver output increases as the pre-emphasis voltage increases, which maintains the same difference between driver current and pre-emphasis current so that the amplitude of signal maximum eye opening is always kept constant.

Figure 10 shows the simulation results for simultaneous bi-directional signaling with and without an adaptive channel pre-emphasis after echo cancellation and pre-emphasis are initialized. It shows that the adaptive channel pre-emphasis helps to open the eye in the VIL(T_O) eye-diagram, which improves the rise and fall times of the received signal.

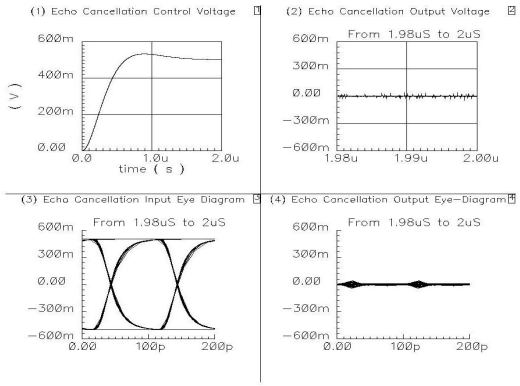

Figure 8. The echo cancellation initialization setup simulation results for the circuits of Figurs 1 and 6.

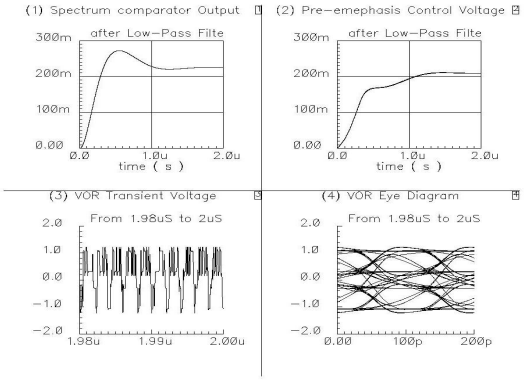

Figure 9. The adaptive channel pre-emphasis initialization setup simulation results for the circuit of Figure 3.

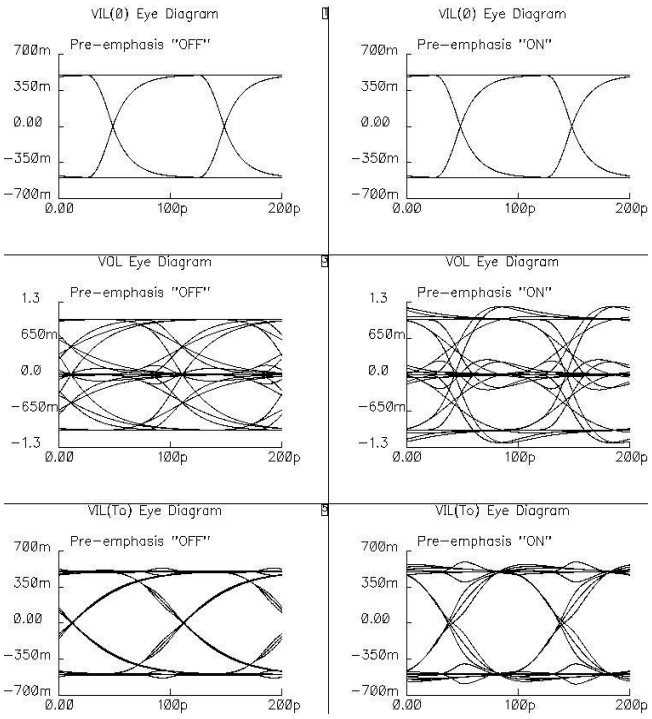

Figure 10. The simulation results for simultaneous bi-directional signaling with and without adaptive channel pre-emphasis after echo cancellation and pre-emphasis are initialized.

4. SUMMARY

This paper presents a novel design for a differential current-mode simultaneous bi-directional signaling system using an adaptive pre-emphasis technique for short distance serial communications. The differential current mode architecture offers insensitivity to common-mode noise, better impedance matching and higher bandwidth performance than other types of systems. Simultaneous bi-directional signaling provides twice the total I/O bandwidth compared to traditional unidirectional signaling. It is most suitable for low loss or short link communications due to the lower voltage margin and higher sensitivity to mismatched impedance. The design incorporates an adaptive equalization approach and it makes use of the inherent feedback loop present in the simultaneous bi-directional link to automatically adjust the amount of pre-emphasis for proper channel loss compensation. The proposed design has been verified with Cadence SpectreRF with Verilog-A simulators. The channel loss characteristic is based on an FR-4 material model which is the standard glass epoxy substrate having approximately 1 dB loss per inch at 10 GHz. The simulation results show that the applied adaptive pre-emphasis for channel loss compensation can dramatically reduce the efforts needed to recover the data at each side of the bi-directional link.

5. REFERENCES

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