# SiGe BiCMOS PAM-4 Clock and Data Recovery Circuit for High-Speed Serial Communications

*Ming-ta Hsieh and Gerald E. Sobelman*
Department of Electrical and Computer Engineering
University of Minnesota
200 Union Street S.E., Minneapolis, MN 55455 USA

## ABSTRACT

A multilevel clock and data recovery (CDR) circuit for high-speed serial data transmission was designed using the IBM 6HP 0.25 μm SiGe BiCMOS process technology. The circuit extracts the clock from a 32 Gb/s 4-level pulse amplitude modulated (PAM-4) input signal and outputs four channels of retimed NRZ data at 8 Gb/s per channel. The CDR design incorporates a PAM-4 to 2-bit-binary converter, a phase/frequency detector, a loop filter, a quadrature LC ring oscillator and a data-retiming module. The circuit operates using a 3.3V supply voltage with a 350mA current consumption. The simulation results show that the peak-to-peak jitter is 1.3 ps, the capture range is 2 GHz, the acquisition time is 200 ns and the input sensitivity is 150 mV. This PAM-based CDR technique is quite suitable for low-loss transmission channels such as fiber optic communications or short-distance copper links, including network-on-chip (NOC) implementations and storage area networks (SANs).

## 1. INTRODUCTION

Many of the high-speed serial data communication systems in use today are based on a binary signaling scheme. For example, optical communication systems use On-Off Keying (OOK), where the presence or absence of a light pulse corresponds to the two possible binary data values. In contrast, in the multilevel data transmission procedure known as PAM-N, a symbol corresponds to one of N distinct amplitude or intensity levels so that each symbol carries $log_2(N)$ bits of information. In this way, the baud rate (i.e., the number of symbols per second) required to send a fixed number of bits per second is lower than for a binary signaling system. This presents an attractive alternative for implementing very high-speed serial data transmission systems, since the front-end transceiver circuits can operate at a reduced clock rate. In particular, PAM-4, PAM-5 and PAM-8 systems have been proposed for use in various copper and optical communications systems [1–4]. However, none of previous works were designed using a BiCMOS process, which has the potential for achieving improved performance.

Clock and data recovery (CDR) is a key block in the receiver which removes unwanted jitter, extracts the clock signal and retimes the received data. In a multilevel system, the design of the CDR presents special challenges since the separation between levels is reduced. As a result, noise margins are of paramount importance and it becomes essential to use an appropriate device and circuit technology. A SiGe BiCMOS process is an ideal choice for this application due to its high cutoff frequency, high breakdown voltage and low noise bipolar devices with compatible CMOS devices and a reasonable cost [5–6].

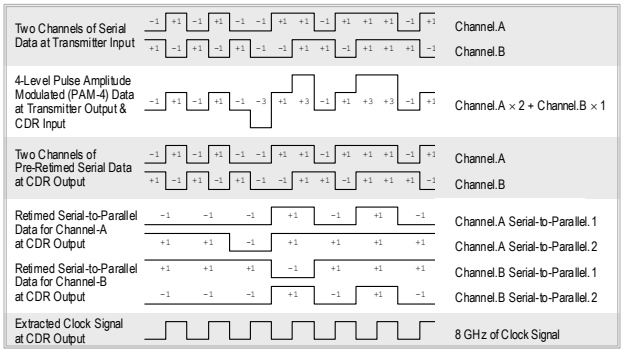


**Figure 1**. Input and output signals for the proposed PAM-4 CDR circuit.

This paper describes a multilevel CDR design based on the IBM 6HP 0.25 μm SiGe BiCMOS process [7] that is available through MOSIS. The CDR accepts a PAM-4 input signal at 16 Gbaud, which is equivalent to a data rate of 32 Gb/s. The transmission occurs at 8 GHz, which is half of the frequency of an equivalent binary data stream. The input and output signals for the proposed PAM-4 CDR are shown in Figure 1. Two channels of serial binary data at the transmitter input are converted into a 4-level pulse amplitude modulated signal at the transmitter output. The PAM-4 signal is sent to the CDR input. The output data is retimed on both edges of clock, which generates 4 channels of parallel output data at 8 Gb/s per channel. Thus, the CDR also provides a built-in 1:4 demux of the 32 Gb/s input signal. The extracted clock for the CDR itself and for receiver system is a set of quadrature signals at 8 GHz. One potential limitation of using a multilevel signaling scheme is the decreased signal-to-noise ratio (SNR). However, this issue can be ameliorated by using appropriate coding and error correction techniques, such as those described in references [8–9].

## 2. MULTILEVEL CDR ARCHITECTURE

The block diagram of the proposed multilevel CDR architecture is shown in Figure 2. (The binary-to-PAM-4 transmitter driver block has been included for built-in self-testing purposes. The pre-emphasis function provides bandwidth compensation for the 32 Gb/s 4-level signal transmission line which might have various length and attenuation characteristics.) The CDR is a phase-locked loop (PLL) based topology which is suitable for data retiming because of its inherent ability to filter input jitter. The PAM-4-to-binary converter module converts the multilevel signal into binary format. A clock generated from the RLC ring

oscillator is used to retime and demultiplex the signal into 4 separate data channels. The phase-frequency detector (PFD) requires quadrature clocks, i.e. having a phase offset of 90 degrees. These are used to distinguish the frequency difference between the data and extracted clocks in the frequency detector module. The loop filter is a low-pass filter which takes the PFD output signal and converts it into a low-frequency signal that drives the RLC ring oscillator.

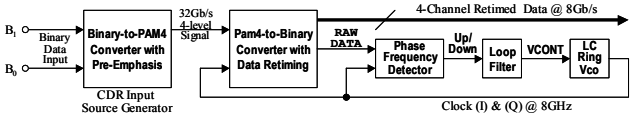


**Figure 2**. The block diagram of the multilevel clock and data recovery architecture.

## 2.1 PAM-4 to Binary Converter

The PAM-4 to binary converter plays a major role in determining the bit error rate (BER) performance of the overall multilevel CDR because of its front-end position. Figure 3 shows the circuit design of PAM-4 to binary converter design. The two pairs of emitter follower, Q1-Q2 and Q3-Q4, perform the 2-bit flash analog-to-digital conversion. The thermometer code output T1 is triggered at the input common-mode voltage. T2 and T0 are triggered at 1/3 of the maximum input signal (peak-to-peak differential) above and below the input common-mode voltage, respectively. Due to the none-zero rise and fall times, the thermometer code outputs T2 and T0 suffer from servere duty cycle distortion. This effect is removed by passing through D-flip-flops before converting to a binary code output.

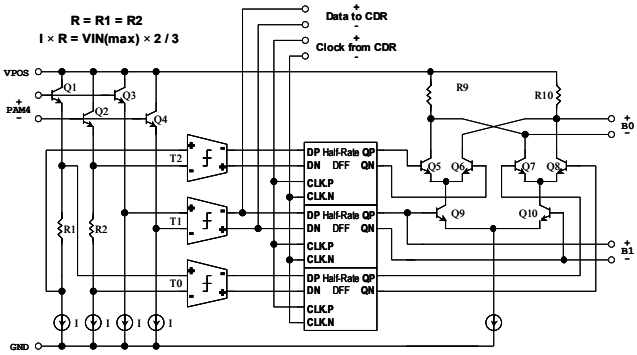


**Figure 3**. PAM-4 to Binary Converter.

## 2.2 Phase Frequency Detector and Loop Filter

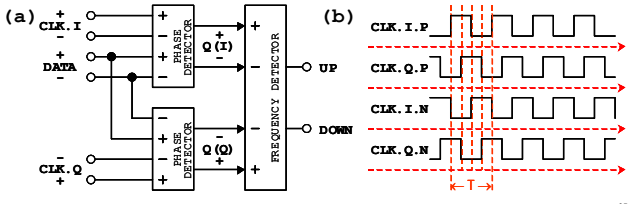


**Figure 4**. Phase Frequency Detector (PFD) (a) Block diagram. (b) Clock signals.

A CDR design that does not use a reference frequency signal normally requires a frequency detector in order to prevent a false lock onto any frequency other than the data frequency. Figure 4 (a) and (b) show the block diagram and clock signals of the phase frequency detector (PFD). The transistor-level implemenation is the one proposed in reference [10]. By using quadrature input clocks for the phase detectors, the relationship between the two phase detector outputs produces a lead or lag signal depending on the sign of the frequency difference between the data and clock. The frequency detector takes output signals from the two phase detectors and generates an up/down signal to indicate the sign of the frequency difference between data and clock. The up/down signal is then used to drive the loop filter.

The loop filter consists of emitter followers at the input, an RC filter and a single-stage differential amplifier with source degeneration. The source degeneration resistor provides linear gain amplification. The basic RC filter with the amplifier was proposed in Reference [12]. The emitter followers at the inputs provide a level shift and an impedance isolation between the PFD and the loop filter. An off-chip filter capacitor is used to adjust the dominant pole location and insert a zero.

## 2.3 LC Ring Oscillator

Several researchers have suggested a combination of ring and LC oscillators to provide wide and fast tuning accompanied with low phase noise and high stability [11]–[12]. Figure 5 (a) and (b) show the circuit implementation of our RLC ring oscillator that has two differential gain stages in the loop and which can exactly generate the quadrature clocks without any extra circuitry. Resistors R1 and R2, together with the parasitic capacitance and gain of the devices determine the oscillation frequency. The inductors L1 and L2 are used to reduce the low frequency components, creating an LC band-pass filter. The frequency control is set by adjusting the tail currents of differential pairs Q3-Q4 and Q5-Q6. The differential pair Q5-Q6 produces a positive feedback which decreases the oscillation frequency as the tail current increases (Q8 turned on).

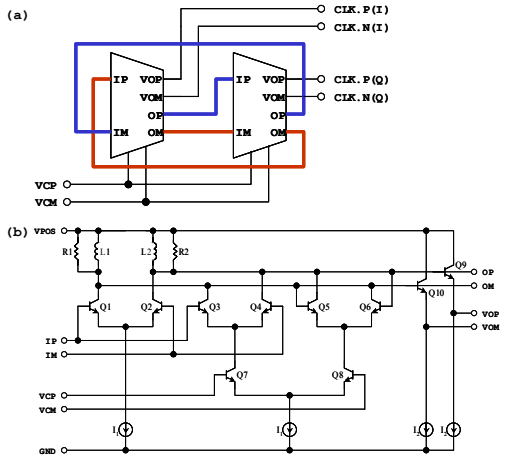


**Figure 5**. Schematic of the RLC ring oscillator. (a) Two-gain-stage ring oscillator. (b) The gain stage circuit.

# 3. SIMULATION RESULTS

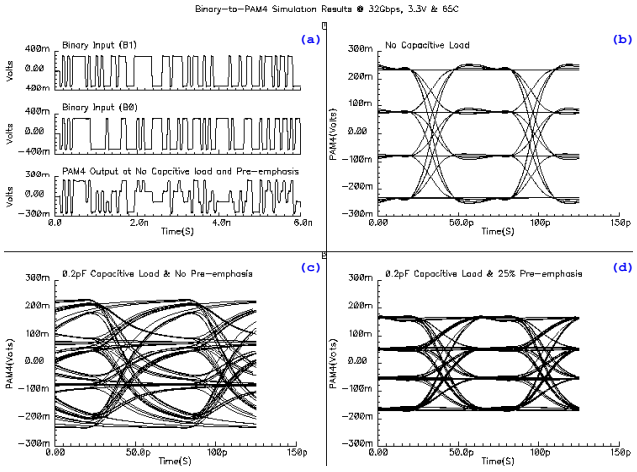


**Figure 6**. Simulation results for the binary-to-PAM-4 converter with or without pre-emphasis at 32 Gb/s (a) Binary input and PAM-4 output transient response. (b) PAM-4 eye diagram with pure resistive load (c) PAM-4 with an additional 0.2 pF capacitive load and no pre-emphasis (d) PAM-4 with extra 0.2 pF capacitive load and 0.25% pre-emphasis.

The simulation results for the binary-to-PAM-4 converter with and without pre-emphasis are shown in Figure 6. Two pseudo-random-binary-sequence (PRBS) generators, B1 and B0, were input and coded into a 4-level signal using a logic circuit and a buffer amplifier as shown in Figure 6 (a) and (b). The comparison for bandwidth limited load between pre-emphasis and no pre-emphasis output is shown in Figure 6 (c) and (d). Due to the bandwidth limited load, Figure 6 (c) shows a closed eye without pre-emphasis. In other words, the characteristics for rise/fall and jitter might not meet the input specification for CDR input. Pre-emphasis has a high-pass characteristic which can cancel out the loss on bandwidth limited load as shown in Figure 6 (d). Both driver and pre-emphasis are bias tail current adjustable. Thus, the output amplitude and the percentage of pre-emphasis can be set independently to compensate for different load characteristics.

Figure 7 shows the simulation results for the phase/frequency detector. When $f_{VCO} > f_{DATA}$, the output of the phase detector leads the output of the quadrature phase detector. This causes the frequency detector to generate a positive control signal to lower the VCO frequency, and vice versa.

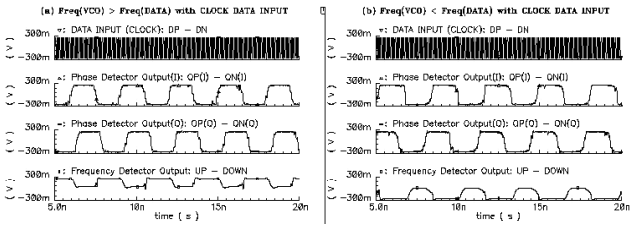


**Figure 7**. PFD at 8 GHz (a) $f_{VCO}>f_{DATA}$ (b) $f_{VCO}<f_{DATA}$

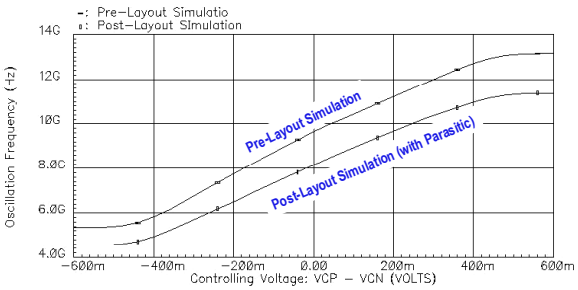


**Figure** 8. RLC ring VCO tuning range pre-layout and post-layout (with parasitic) simulation.

Figure 8 shows RLC ring VCO tuning range pre-layout and post-layout (with parasitic) simulation. Due to the parasitic capacitance and resistance on the chip, the VCO pre-layout simulation must have oscillation frequency slightly higher than the desired frequency range. The simulation results show the tuning range is more than 4 GHz.

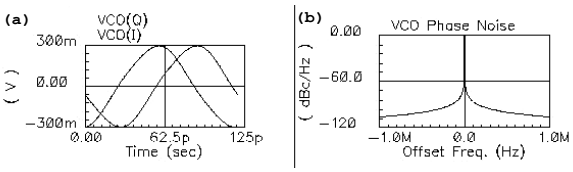


**Figure** 9. RLC ring VCO simulation results (a) Transient response of VCO quadrature output. (b) VCO phase noise vs. offset frequency.

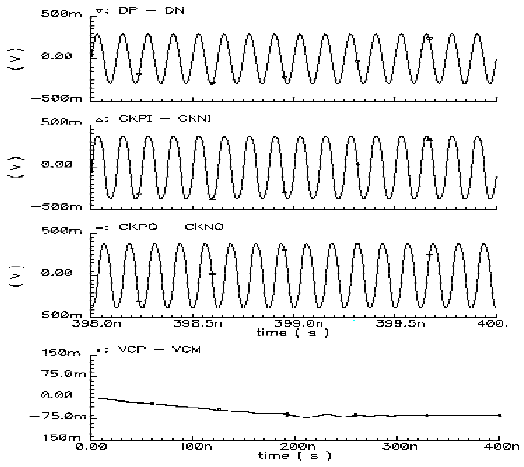


**Figure 10**. Simulation results of VCO control voltage and clock output during the phase locked loop lock-in process.

Figure 9 (a) shows the transient response of the quadrature outputs. The phase noise versus offset frequency in Figure 9 (b) shows the low phase noise of the design, which arises from the use of the inductor in the ring oscillator. Figure 10 shows the control signal (VCP – VCM) during the lock-in process of the phase locked loop. The data signal (DP – DN) is aligned with CKP.I – CKN.I and is shifted by 90 degrees from CKP.Q – CKN.Q.

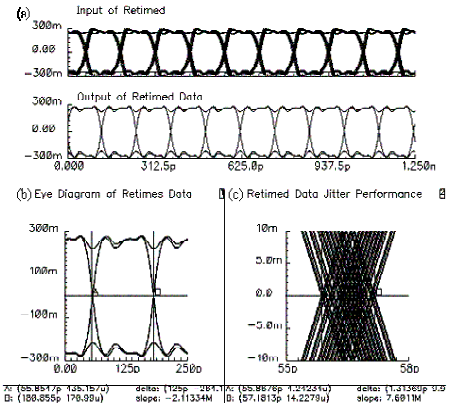


**Figure 11**. Retimed Data. (a) Input and Output in Superposition. (b) Eye Diagram of Output Retimed Data. (c) Retimed Data Jitter Performance (Typical).

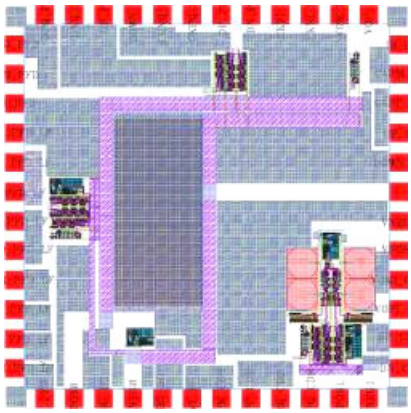

**Figure 12**. Layout plot of the multilevel CDR design.

Figure 11 shows the input signal and output retimed data as well as the jitter performance for typical conditions. The final output consists of 4 channels of 8 Gbps signals. The simulated peak-to-peak jitter is found to be 1.3 pS. The final layout plot of this multilevel CDR design is shown in Figure 12.

## 4. SUMMARY

A PAM-4 clock and data recovery circuit for multilevel communications systems was designed using a 0.25µm SiGe BiCMOS process. The input takes a 4-level PAM signal at 32 Gb/s and converts it into four channels of 8 Gb/s data. Such a multilevel data transmission system provides an opportunity to increase the data transmission rate with minimized cost and only a few additional components. The proposed design uses a differential input adapter technique to implement the high-speed differential PAM-4 ADC at the front-end of the system. The phase/frequency detector design eliminates the need for an external reference frequency. The VCO provides wide and fast tuning along with low phase noise and high stability due to the LC tank and ring oscillator.

## 5. ACKNOWLEDGEMENTS

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## 6. REFERENCES

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