

Design of a High-Performance Scalable CDMA Router for On-Chip Switched Networks

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Abstract – Performance results and synthesized area overhead for a code division multiple access (CDMA) router intended for network-on-chip (NoC) applications are presented. Specific architectural block diagrams of the main components of the router are given and synthesis results are provided for 0.18 micron and 0.25 micron structured ASIC libraries. Post-synthesis VHDL simulations verify the functionality of the router and provide values for packet transmission latency and throughput as functions of the payload size. The router can be used to construct star+star and star+mesh network architectures which can be scaled to meet the needs of high-performance applications.

Keywords: router, CDMA, network-on-chip

1 Introduction

Future system-on-chip (SoC) designs will have hundreds of intellectual property (IP) blocks on a single chip. Based on the semiconductor industry association (SIA) road map [1], by the end of the decade SoCs designed using 50nm technology will have up to 4 billion transistors running at 10GHz [2]. The on-chip communication requirements for these systems are very demanding because many or all of those IPs need to communicate in the Gbps range. In particular, concerns related to the interconnections and their delays [4] have given rise to router-based on-chip interconnects, also known as network-on-chip (NoC) or on-chip switched network (OCSN) architectures. The design of such scalable and modular high performance router-based on-chip networks are crucial to the success of this NoC design paradigm.

NoCs provide a way to overcome the limitations inherent in traditional bus-based interconnection schemes [2, 3]. NoCs can have the following benefits: (a) throughput increase via high performance switching technology, (b) lower energy dissipation, (c) flexible scalability and (d) design reusability. On the other hand, the routers require a certain amount of overhead. Therefore, it is important to determine the area overhead that is required so that the cost and performance trade-off between bus-based and NoC-based designs can be understood.

CDMA techniques are widely used in wireless commu-

nications systems. Recently, some researchers have proposed various ways of applying CDMA to wired communications environments. References [5, 6] develop a bus interface which features multi-bit simultaneous data transmission and multi-valued CDMA techniques for higher bandwidth, but these did not consider a packet-based network approach. The paper of Bell et al [7] proposed a method using pseudo-noise (PN) sequences to route packets between processors in a multi-processor network. However, it used only one large central switching element to perform all of the routing and did not consider issues such as buffering, packet contention or the on-chip environment in which some of the resources may not be generating traffic at certain times.

Our CDMA-based router is developed to address NoC applications. It can seamlessly handle situations in which some of the resources do not have any data to send during a given packet interval. The implementation uses traditional binary signaling and includes capabilities for packet buffering and contention resolution. This paper describes the detailed register-transfer level design of the components within the routers and presents synthesis results to determine its performance and area overhead. Synthesis was performed using the Synplify ASIC 3.3 tool with the Chip Express CX5000 and CX4000 structured ASIC libraries for 0.18 μ m and 0.25 μ m technologies, respectively [11]. We show how the router is easily scalable and how it can be applied to other types of NoC topologies. Also, the CDMA router-based star+star and star+mesh on-chip network topologies have a better value for the ratio of the number of resources to the number of routers compared to the general crossbar switch topologies.

2 CDMA Router Architecture

The architecture of the CDMA-based router is presented in Figure 1. It is composed of seven functional modules: FIFO buffer, Walsh codeword storage, header decoder, scheduler, modulator, code adder and demodulator. The resources attached to the router can be any type of digital IP modules that may be found in an SoC such as a processor, memory, DSP core, controller or other specialized logic blocks.

Data is transferred from one resource to another using a

packet format, which is divided into three fields: 3-bit source address, 3-bit destination address and parameterizable size of payload. We assign seven of the eight available non-zero 8-bit Walsh codewords to seven attached IP resources, reserving the all-zero codeword for use in the case where no data is to be sent. Larger routers can be constructed using larger codeword sets. For example, if we use 16-bit Walsh codewords, then the number of IP resources attached to each router can be extended up to 15. The router can support a large aggregate data throughput because all resources can simultaneously send packets to their destination due to the orthogonality of the Walsh codewords. Our CDMA router is modular and reusable, and this leads to a very regular and predictable communications infrastructure which can be used in a wide range of design applications.

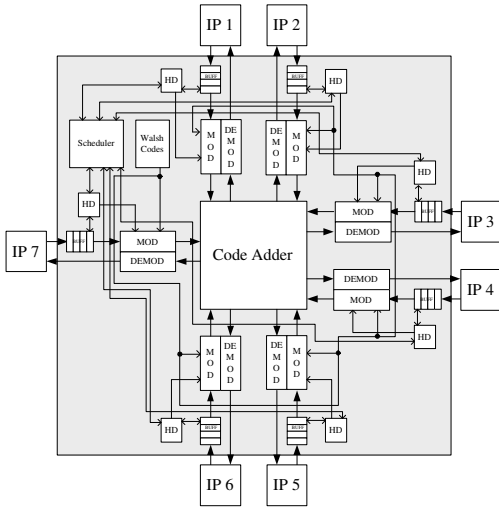


Figure 1: CDMA router architecture.

2.1 Modulator

The grant signal from the header decoder causes a packet in the buffer to be forwarded to the Modulator (MOD), where the corresponding Walsh codeword is selected. The codeword is modulated with each bit of the packet in a parallel fashion via MUXes as shown in Figure 2. The modulation algorithm is described in Table 1, which illustrates how the assigned destination-oriented codeword is modulated in terms of the original data.

Table 1: Modulation algorithm

Data	Codeword Assignment
0	Codeword itself
1	Inverted codeword
No data	All-zero codeword

2.2 Demodulator

The demodulator (DEMOM) recovers the original data from the summation value produced by the code adder. It

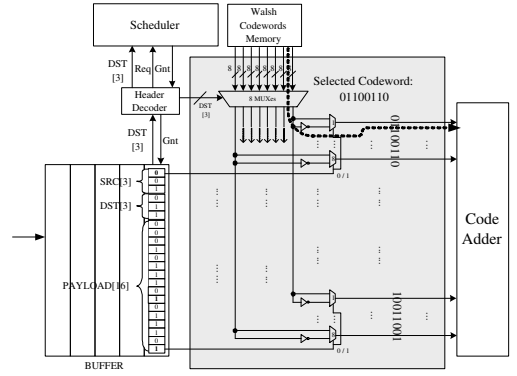


Figure 2: Modulator block diagram.

uses the decision factor λ , which is a modified form of the calculation in [7] to make our algorithm work with Walsh codes.

The mathematical equations and algorithms necessary for demodulation are summarized below and in Table 2.

$$D[i] = \begin{cases} (2S[i] - L) & \text{if codeword}[i] \text{ is } 0 \\ (-2S[i] + L) & \text{if codeword}[i] \text{ is } 1 \end{cases} \quad (1)$$

$$\lambda = \sum_{i=0}^{L-1} \frac{D[i]}{L} \quad (2)$$

- L is the codeword length.
- $D[i]$ is the decision variable.
- λ is the decision factor.

Table 2: Demodulation algorithm

Decision Factor(λ)	Demodulated Data[bit]
+1	1
-1	0
0	No data sent

3 Scalable CDMA-based NoC

The router is easily scalable by simply using a longer size of Walsh codewords. If we use 16-bit and 32-bit Walsh codewords, then the number of IP resources attached to each router can be extended easily up to 15 and 31, respectively. Moreover, as shown in Figure 3 and Figure 4, one CDMA router with its attached IP blocks can be hierarchically extended to construct larger NoC topologies. Figure 3 shows the hierarchical star+star on-chip topology that interconnect each group of local CDMA routers with IP blocks through a CDMA central router, using a specific packet format. In this case, a group field to distinguish each local switch group should be included in the packet format for the simultaneous packet transmission via the central router. Figure 4 shows

an alternative topology in which each router group is interconnected using a mesh structure. This hybrid topology has a better resource to router ratio compared to a pure mesh topology NoC [3]. Table 3 summarizes the overall comparison to other types of the on-chip topologies in terms of hop count, resource to router ratio, routing overhead, wire length overhead and wiring complexity.

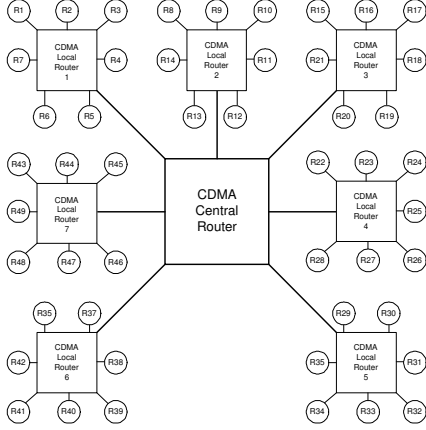


Figure 3: Scalable CDMA star+star topology.

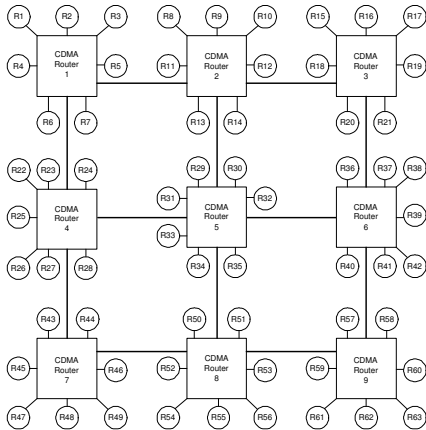


Figure 4: Scalable CDMA star+mesh topology.

4 Synthesis Results and Analysis

In this section we give the implementation results for our CDMA router. We have used the Chip Express CX4000 and CX5000 structured ASIC libraries for $0.25\mu\text{m}$ and $0.18\mu\text{m}$ technologies, respectively, and synthesized with the CAD tool Synplify ASIC 3.3. The architecture overhead is determined in terms of gate count and area. The design was successfully simulated and verified with the ModelSim simulator using the post-synthesis netlist and randomly generated traffic patterns. The results provide values for the aggregate throughput and the packet transmission latency as a function of packet size, which are the performance metrics of interest.

The synthesis results for both $0.25\mu\text{m}$ and $0.18\mu\text{m}$ technologies are presented in Table 4 and Table 5. We list the op-

timal estimated frequency to avoid negative slack, total number of gates and the area for the various payload size from 8 bits to 128 bits. The optimal estimated frequency range of the $0.25\mu\text{m}$ and $0.18\mu\text{m}$ technologies are around 50MHz and 94MHz, respectively.

Table 4: Synthesis area report for $0.25\mu\text{m}$

0.25 μm ChipExpress cx4001 structured ASIC library				
Payload [bits]	Optimal Estimated Frequency	Optimal Estimated Period	Cell Usage	
			Gate Count	Area [μm^2]
8	50.0 MHz	20.005 ns	17838	39304.2
16	49.4 MHz	20.223 ns	27153	59780.5
32	50.0 MHz	20.005 ns	44314	99480.8
64	50.0 MHz	20.000 ns	81266	181060.0
128	50.0 MHz	19.997 ns	160906	354877.0

Table 6 shows detailed area overhead of each CDMA NoC router component within a CDMA NoC router for the case of an 8-bit payload size in $0.25\mu\text{m}$ technology. From the result, the things we should note are: First, we can see the demodulation part has the largest area overhead amongst all of the components. This is expected due to the computational complexity of that part of the algorithm. Second, the area of the $0.18\mu\text{m}$ technology is 34% on average smaller than the area of $0.25\mu\text{m}$ technology while the gate counts are almost the same.

Table 5: Synthesis area report for $0.18\mu\text{m}$

0.18 μm ChipExpress cx5000 structured ASIC library				
Payload [bits]	Optimal Estimated Frequency	Optimal Estimated Period	Cell Usage	
			Gate Count	Area [μm^2]
8	94.9 MHz	10.539 ns	19416	26390.0
16	94.7 MHz	10.560 ns	29113	39736.0
32	94.2 MHz	10.615 ns	47754	65746.0
64	93.8 MHz	10.660 ns	86912	119000.0
128	93.4 MHz	10.706 ns	167740	2284480.0

While the area overhead of modulator, buffer, code adder and demodulator increase as the packet size increases, the scheduler and the header decoder keep the same area overhead regardless of packet size, since these are only functions of the number of attached IP resources.

Figure 5 shows the maximum aggregate throughput values of a 7-port CDMA NoC router for different payload sizes in $0.25\mu\text{m}$ and $0.18\mu\text{m}$ technologies, respectively. The throughput values, in bits per second, can be computed for each payload size by forming the following product: (7 IP resources)*(number of payload bits)*(clock frequency). (Note that we assume that the interconnections between the IP resources and the router are parallel paths whose width is equal to the total packet length). Therefore, we arrive at throughput values up to 44.8Gbps and 83.7Gbps for the case of 128-bit payload size in $0.25\mu\text{m}$ and $0.18\mu\text{m}$ technologies, respec-

Table 3: Performance comparison of the different network-on-chip topologies

Topology	Sum of Resources (RSC)	Sum of Routers (RTR)	Min. Hop Count	Max. Hop Count	RSC/RTR Ratio	Routing Complexity Overhead [8]	Wire Length Overhead [8]	Wiring Complexity Overhead [8]
Mesh [3]	64	64	2	15	1	Medium	Low	Low
Fat-tree [9]	64	48	1	3	0.75	High	High	High
Butterfly Fat-tree [10]	64	28	1	5	0.44	High	High	High
CDMA Star+Star	49	8	1	3	0.16	Low	Low	Low
CDMA Star+Mesh	63	9	1	5	0.14	Medium	Low	Low

tively. In addition, simulation results in the same value for packet latency of 160 ns since each bit of the packet is transmitted in parallel.

Table 6: Components area overhead

Components area overhead of 8 bits payload case in 0.25 μm technology	
Components	Area [μm^2]
Modulator (MOD)	3930.4
Buffer (BUFF)	6681.7
Header Decoder (HD)	432.4
Scheduler (SCHE)	786.1
Code Adder (CA)	2358.2
Demodulator (DEMODO)	24761.6
Others	353.8
TOTAL	39304.2

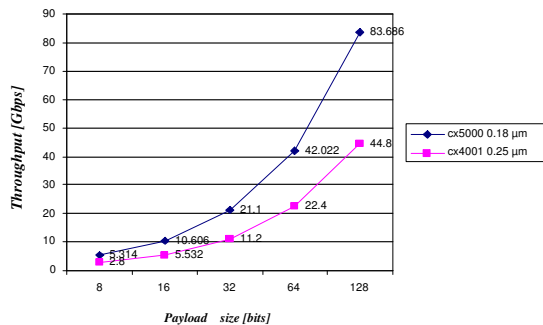


Figure 5: Throughput performance [Gbps].

5 Conclusions

We have presented the detailed design and synthesis results of a CDMA-based NoC router architecture. The system has been modeled with VHDL and successfully synthesized using 0.18 μm and 0.25 μm structured CMOS ASIC technologies. The CAD tool Synplify ASIC 3.3 was used to perform the synthesis, and gate count and area results have been tabulated. Simulation results verify the function of the proposed CDMA algorithm and provide values for the aggregate throughput for various payload sizes as well as the packet transmission latency. In our future work, we plan to model an MPEG-4 system to determine its performance using this

NoC approach. In addition, we intend to investigate the use of more sophisticated scheduling algorithms.

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