CDMA-BASED NETWORK-ON-CHIP ARCHITECTURE

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ABSTRACT

We present a novel Network-on-Chip (NoC) architecture that is based on Code Division Multiple Access (CDMA) techniques. The orthogonality properties of a Walsh code are used to route data packets between resources. A star network topology allows a hierarchical switching platform to be constructed which can be scaled to handle large systems. The switching element and network topology are described and algorithms for modulation and demodulation of packets are presented. Simulation results for throughput and latency are given.

1. INTRODUCTION

The Network-on-Chip (NoC) concept has recently become a widely discussed technique for handling the large on-chip communication requirements of complex System-on-Chip (SoC) designs [1]. A traditional bus-based interconnection scheme does not scale well to very large SoCs because many Intellectual Property (IP) blocks must contend with each other to communicate over the shared bus. In contrast, an on-chip network uses the packet-switching paradigm to route information between IP blocks and it can be scaled up to achieve a very large total aggregate bandwidth within the chip.

Several researchers have recently proposed various types of NoC implementations [2, 3, 4]. In this paper, we propose a new type of NoC which is based on using Code-Division Multiple Access (CDMA) techniques. CDMA has been widely used in wireless networks but has only been rarely applied to implement wired networks. The paper of Bell et al [5] proposed using PN sequences to route packets between processors in a multi-processor network. However, it used only one large central switching element to perform all of the routing and did not consider isssues such as buffering and packet contention. Furthermore, it was not specifically targeted at the NoC environment. Other papers have considered multi-valued (i.e., non-binary) signaling with CDMA to increase bus bandwidth [6, 7, 8], but these did not use a network architecture and relied on non-traditional signaling methods. In contrast, our approach constructs a switched network architecture using traditional binary signaling and includes capabilities for packet buffering and contention resolution that are targeted specifically for NoC applications. We propose a star network topology that is well matched to our basic CDMA switching element and which can be hierarchically scaled to handle a large number of IP blocks. Our NoC architecture has been simulated using SystemC and we give results for the throughput and latency of various network configurations.

2. CDMA-BASED SWITCH ARCHITECTURE

The block diagram of our CDMA-based switching element is shown in Figure 1. This local switch can be used to connect up to as many as 7 resources, i.e. 7 different IP blocks. A very similar switching element is also used as the central switch in our star-based network topology. The various aspects of the switch design and operation are presented in the following subsections.

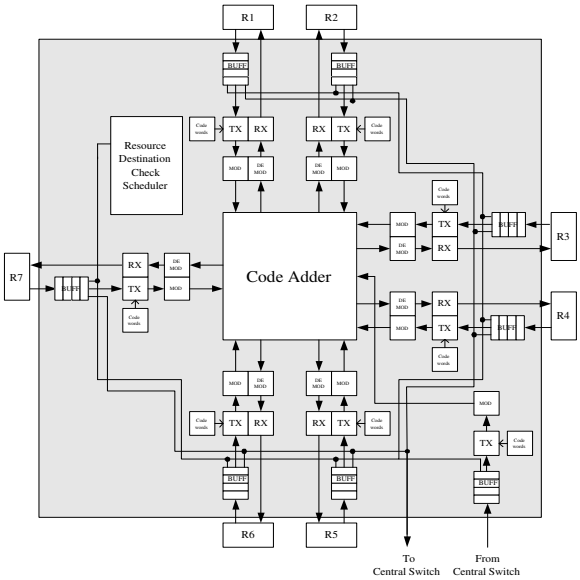

Fig. 1. Block diagram of the CDMA switch.

2.1. Packet Structure

Each packet is divided into five fields. A valid bit indicates if the payload consists of actual information or null data. This allows the system to handle situations in which a resource does not have any information to send to another resource. A group field is used to identify each local

switch group. It is used to determine whether a packet is destined for a resource within the local switch group or if it is for a resource belonging to another local switch group. A source address field and a destination address field are included and the payload consists of a fixed number of bits. In our simulations, we have experimented with several different fixed payload sizes ranging from 8 bits up to 40 bits.

2.2. Walsh Code Generator

The spreading code used in our design is the 8-chip orthogonal Walsh code. Each of the 7 resources connected to a local switch is associated with one of the 7 non-zero Walsh codewords. The Walsh code generator produces these codewords.

2.3. FIFO Buffer and Scheduler

While many network switches use output buffering to avoid head-of-line (HOL) blocking, we have adopted input buffering in this design. Input buffering normally has a lower complexity and consequently a lower cost of implementation. Also, the switch fabric and the memory at the inputs of an N-by-N input-queued switch need only run as fast as the line rate, whereas output buffering has to run N times as fast as the line rate. The width of each buffer is equal to the packet length and the each buffer holds four packets. Store-and-forward routing is used for its simplicity of implementation.

Whenever destination contention is detected, we use a priority scheme which is based on the resource number that an IP block occupies at the switch: higher resource numbers have higher priority. While this is not a fair scheduling scheme, it is simple and does not require much hardware overhead for its implementation. Moreover, in many applications, traffic to some IP blocks would normally be of higher priority than others and this can be enforced by simply assigning those IP blocks to the highest number switch input.

2.4. TX and MOD

The TX block receives a packet from the buffer and examines its destination field. TX then selects the Walsh codeword that corresponds to this destination. The MOD block modulates the payload bits with the selected codeword. In other words, each payload bit is spread by modulation with the codeword. The specific form of CDMA modulation that is used is given in Algorithm 1.

Algorithm 1 Modulation Algorithm

if data is 0 **then**
  assign codeword itself
else if data is 1 **then**
  assign inverted codeword
end if

2.5. Code Adder

All of the modulated data from the seven resources are summed together in the code adder. The summation range of each codeword chip is thus from 0 to 7. The summation result is then sent to the demodulator.

2.6. DEMOD and RX

The demodulator recovers the original data from the summed and spread data. We use the decision variable 2P-N of Ref. [5], where P indicates the sum of all modulated value and N indicates the number of bits of the codeword. The details of the demodulation procedure are given in Algorithm 2 and one specific demodulation example is illustrated in Figure 2. In the example, assume that resource 4 (R4) wants to send a bit 0 with Walsh code C4, which is [0 0 0 0 1 1 1 1], and that the other six resources also send 0 or 1 simultaneously in a similar manner. After the code adder sums all of the modulated signals coming from all seven resources, the summed value P is [3 0 3 2 2 3 4 3]. The demodulator module first doubles each digit, resulting in [6 0 6 4 4 6 8 6]. The bits of codeword X[i] determine how the decision will be made. If the bit of the codeword is '0', 2P-N is used for the decision, whereas -2P+N is used when the codeword bit is '1'. In our example, these steps would result in [-2 -8 -2 -4 4 2 0 2].

Then, upon adding up all of these values, we have a result of -8, which we divide by N, i.e. 8 in our case. Therefore, the final value is -1. From the demodulation algorithm, we would correctly determine that the original data was a '0' because λ is equal to -1. By repeating this process, we can recover all of the original data that was sent.

Algorithm 2 Demodulation Algorithm

Let

$$X[i] = \begin{cases} (2P - N) & \text{if codeword}[i] \text{ is 0} \\ (-2P + N) & \text{if codeword}[i] \text{ is 1} \end{cases} \quad (1)$$

Where N is the size of codeword
and P is the sum of all the modulated values.

Let

$$\lambda = \sum_{i=0}^{N-1} \frac{X[i]}{N}$$

if $\lambda = 1$ **then**
  demodulated data is value 1
else if $\lambda = -1$ **then**
  demodulated data is value 0
end if

During the demodulation process, the RX module waits until one complete packet has been completely demodulated. After the entire payload is available, it is then delivered as a unit to its intended resource.

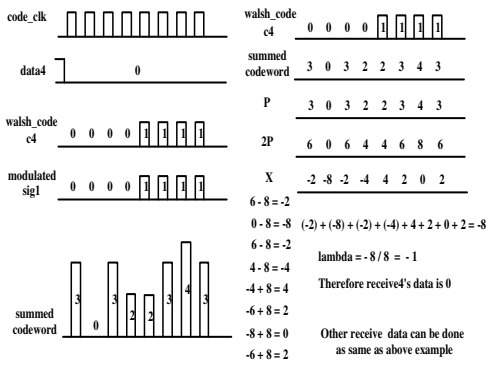

Fig. 2. Demodulation example.

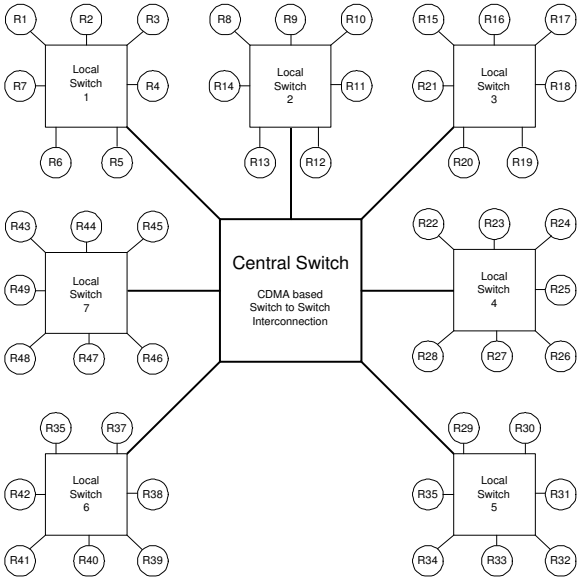

Fig. 3. CDMA star NoC topology.

3. NETWORK-ON-CHIP ARCHITECTURE

The hierarchical star interconnection network topology that we use in this research builds on our basic local switch design and provides efficiency, flexibility and scalability for the total network architecture.

When a resource wants to send a packet to another resource residing in a different local switch group, the packet is transmitted through the central switch. As shown in Figure 3, we can see that each local switch is attached to the central switch in a manner similar to the way in which IP blocks are connected to a local switch. Likewise, a distinct non-zero codeword is assigned to each local switch that connects to the central switch. Therefore, up to 7 local switches can be connected to one central switch in the two-level star topology that is shown.

Table 1 shows the number of resources per switch for several proposed types of NoC topologies. The table indicates that the CDMA star topology has the most favorable (i.e., lowest-overhead) value of this metric.

The size of our CDMA star network can be expanded in two ways. First, we can add additional levels to the hierarchy so that several central switches are connected to a higher-level master switch, and so on. In that type of configuration, additional fields would have to be added to the packet header to correspond to the new levels of the hierarchy. In addition, if we use a larger Walsh code such as the 16-chip code, then the number of objects attached to each switch can be extended to 15. Furthermore, all of the local, central and master switches can be designed as reusable IP blocks and the various network configurations can be fully pre-characterized in terms of their speed, power and area requirements.

	Attached Units	switches	S/U Ratio
mesh[3]	64	64	1
tree	64	63	0.98
fat-tree[9]	64	48	0.75
butterfly-fat-tree[10]	64	28	0.43
CDMA star	42	8	0.19

Table 1. Attached units vs. total number of switches.

Packet Size	Throughput [packets/s]	Latency [ns]
24	182M	22.6
36	121M	28.4
48	91M	36.2
56	78M	44.8

Table 2. Simulation results.

4. SIMULATION RESULTS

We have simulated our entire architecture using SystemC. The performance metrics that we have analyzed are throughput and latency as a function of the number of attached local switches. Seven resources are attached to each local switch and seven local switches communicate with each other via one central switch. In our simulations, all of the data was randomly generated and we set the resource clock period to N times the codeword clock, i.e. $T_{sys\_clk} = N * T_{code\_clk}$. The demodulator outputs the recovered data after three system clock cycles for traffic within the same local switch and after eleven system clock cycles for traffic between different local switches. Therefore, $T_{one\_packet\_delivery} = Packet\_length * T_{sys\_clk} + 3 * T_{sys\_clk}$ within a local switch and $T_{one\_packet\_delivery} = Packet\_length * T_{sys\_clk} + 11 * T_{sys\_clk}$ between different local switches through the central switch. The data in the Table 2 is the average value of these two cases. Throughput is computed as the ratio of the number of transferred packets per unit time. In order to see how the fixed packet size affects system performance, we have run simulations over a range of values for the fixed packet size between 24 and 56 bits, which corresponds to a payload size of between 8 and 40 bits.

5. CONCLUSIONS

In this paper, a new CDMA-based on-chip interconnection network has been presented. Walsh codes are used to modulate the packet data and a hierarchical star network configuration is scalable to handle a large number of communicating IP blocks. Simulations have been performed using SystemC which show good results for throughput and latency.

The CDMA approach provides an effective, low-overhead method for implementing high-performance NoCs and presents many opportunities for further investigations and optimizations. In our future work, we plan to investigate other possible network topologies as well as more sophisticated schemes for buffering and priority/contention resolution.

6. ACKNOWLEDGEMENTS

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