

DIGIT-SERIAL MULTIPLIER DESIGN USING SKEW-TOLERANT DOMINO CIRCUITS

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ABSTRACT

A novel connection between digit-serial computing and skew-tolerant domino circuit design is developed and applied to the design of unsigned and signed multipliers. In our design methodology, a multiplier having a digit size of N bits is naturally and efficiently mapped into a skew-tolerant domino implementation using N overlapping clock phases. In order to demonstrate the performance advantage of our approach, we compare two types of multiplier implementations, one constructed using traditional domino circuits and the other using the skew-tolerant domino technique. The simulation results show that a particular digit-serial multiplier constructed with skew-tolerant domino circuits is up to 41% faster than the corresponding design with traditional domino circuits.

1. INTRODUCTION

Digital signal processing (DSP) is used in a wide range of applications including audio and video compression, wireless communications, etc. DSP hardware nearly always requires the efficient implementation of multiplier units. Many bit-serial and bit-parallel multiplier designs have been proposed for use in DSP applications. However, bit-serial systems may be too slow and bit-parallel systems may be faster than necessary and occupy a considerable amount of area. Digit-serial designs have been proposed as a way to avoid the disadvantages of bit-serial and bit-parallel systems. Several previous digit-serial multiplier designs have been presented in the literature [1], [2], [3], [4], [5]. Most of these implementations use static CMOS logic circuits.

In recent years, domino logic has become a popular alternative for high-speed circuit design. However, the traditional domino clocking scheme [6] uses two-phase clocking with intermediate latches and suffers from several significant sources of clocking overhead such as clock skew, latch delay, and imbalances in the delays in different blocks. Skew-tolerant domino circuits [7] make use of multiple-

phase overlapping clocks in such a way that all of the overhead associated with the traditional domino clocking can be eliminated, and this can result in a significant performance improvement. In this paper, we present a novel digit-serial multiplier structure built with skew-tolerant domino circuits which fully utilizes the speed advantage of domino circuits. Moreover, we will show that there is a natural mapping of digit-serial data paths onto skew-tolerant domino circuits that leads to efficient design implementations.

This paper is organized as follows: In Section 2, we briefly review the concepts of skew-tolerant domino circuit design. The basic principles of bit-serial multiplier design are described in Section 3. Then, in Section 4, we present unsigned and signed digit-serial multipliers having a digit size of N bits that are implemented using skew-tolerant domino circuits with N overlapping clock phases. Comparisons between the skew-tolerant and traditional domino circuits are presented in Section 5, and the main conclusions of the paper are summarized in Section 6.

2. SKEW-TOLERANT AND TIME-BORROWING DOMINO CIRCUITS

Many digital systems are constructed using static CMOS logic gates and edge-triggered flip-flops, but these designs may have limited speed and suffer from overhead such as clock skew, flip-flop delay, and imbalances in the delays in different blocks. Domino logic has become a popular alternative for high speed circuit design because domino CMOS gates are generally faster than static CMOS gates. Traditional domino circuit design uses two-phase clocking in which the precharge and evaluation of adjacent logic blocks occur on alternate phases and where the intermediate results are stored in mid-cycle latches. However, these implementations also suffer from a significant clocking overhead due to skew, latch propagation delay, and imbalanced propagation delay, as illustrated in Figure 1(a). On the other hand, skew-tolerant domino circuits, a recently introduced

method of controlling domino gates with multiple, overlapping clock phases, may eliminate all sources of overhead and thereby offer significant performance improvement. A four-phase overlapping clock scheme with 50% duty cycle phases is shown in Figure 1(b). One of the benefits of this approach is the fact that intermediate latches are not used, so that time borrowing can occur between adjacent phases. In the event of clock skew, the time when two adjacent clock phases are high can be used to provide clock skew tolerance and/or time borrowing. Thus, skew-tolerant domino circuits eliminate latch propagation delay, provide immunity to clock skew and manage imbalances in the logic by allowing time borrowing to occur. Therefore, they allow the speed advantage inherent in domino logic circuits to be fully utilized.

In this paper, we will show how N overlapping clock phases can be used to design unsigned and signed digit-serial multipliers having a digit size of N bits. This provides a natural mapping of digit-serial data paths onto skew-tolerant domino circuits and leads to fast and efficient design implementations.

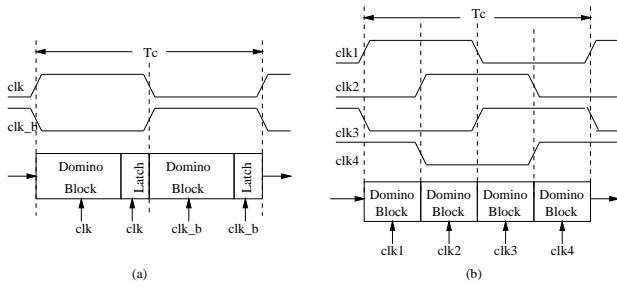


Fig. 1. Skew-tolerant and traditional domino clocking schemes. (a) Traditional two-phase clocking. (b) Four-phase overlapping clocking.

3. BIT-SERIAL MULTIPLIER IN STATIC CMOS

As a preliminary step to the digit-serial designs, we briefly review the structure of a conventional unsigned bit-serial multiplier having a word size of 4 bits. The design is achieved by folding the rows of a parallel multiplier into a single row and inserting delay elements, as shown in Figure 2(a). Figure 2(b) shows the logic function corresponding to Cell-A, which is composed of a full adder and an AND gate. In this structure, the bits of the multiplicand, A , are applied in parallel, with the least-significant-bit (LSB) on the right. The bits of the multiplier, B , are input serially, with the LSB first. The product, out , is produced one bit per clock cycle, with the LSB first. During the computation, each bit of the partial product is added together with the appropriate previous sum (So) and carry-out (Co) bits. The multiplier, B ,

must be extended by adding four extra zero bits in order to obtain a complete 8-bit product in 8 clock cycles.

In our design approach, this basic structure will be extended to the digit-serial case in the following way: One bit will be utilized in each of N clock phases, so that an entire N -bit digit can be processed in one full clock cycle. A skew-tolerant domino implementation will provide the N overlapping clock phases, so that time borrowing and skew-tolerance can be achieved.

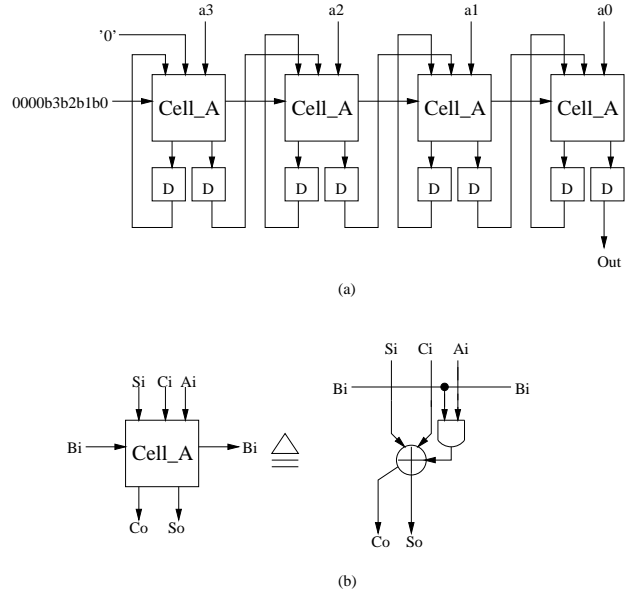


Fig. 2. Structure of a bit-serial multiplier. (a) Top-level design. (b) Logic function for Cell-A.

4. DIGIT-SERIAL MULTIPLIERS USING SKEW-TOLERANT DOMINO CMOS

In digit-serial computation, data words of size W bits are partitioned into digits of size of N bits and are processed serially one digit at a time, with the least significant digit (LSD) first. In this section, we will present unsigned and signed digit-serial multipliers having a word size of 16 bits and using a digit size of 4 bits.

4.1. Unsigned Digit-Serial Multiplier

A 16-bit unsigned digit-serial multiplier with a digit size of 4 bits and a 4-phase overlapping clocking scheme is shown in Figure 3(a). The design is composed of three components, called Block-A, domino buffer, and MUX. All three components are implemented using dual-rail domino CMOS circuits. Block-A is constructed using a partial product generator and a carry save adder (CSA), as shown in Figure 3(b). One clock cycle is composed of 4 overlapping 50%

duty cycle phases called CLK1 - CLK4, where each phase is offset by one-quarter cycle from the previous phase. The multiplicand, A , is applied as a parallel word and the multiplier, B , is partitioned into 4-bit digits, with the LSD first. During the first clock cycle, the carry-in bits and the sum-in bits in the first block load zeros as the initial value through the MUX. After one clock cycle, the carry-out bits, $tc4$ and the sum-out bits $ts4$ are fed back to the carry-in bits and sum-in bits for next multiplication and the 4-bit product, $out(3 : 0)$ is generated on the right, LSD first. Domino buffers are used instead of latches between phases to hold the result ($out(0) - out(2)$) before it is lost to precharge. After the first 4 clock cycles, the entire 16 bits of the B operand have entered the multiplier and the low-order four digits of the product are produced at the output. The remaining high-order 4 digits of the product are obtained by inserting zeros into the $b(3 : 0)$ inputs during each of the second set of 4 clock cycles. Thus, a complete 32-bit product is obtained in 8 full clock cycles. In general, for the case of a $W \times W$ -bit digit-serial multiplier with a digit size of N bits, $2W/N$ clock cycles would be required in order to obtain the full-precision result.

We have compared two 16-bit unsigned digit-serial multipliers, one constructed using traditional two-phase non-overlapping domino with latches and the other using 4-phase skew-tolerant domino. All simulations have been performed using a 0.25 micron TSMC CMOS technology with a supply voltage of 2.5V, under nominal process and environmental conditions. Figure 4 shows the simulation results for one full clock cycle. The traditional two-phase clocking wastes some time due to imbalanced logic delays in different blocks as well as in the required latch propagation delay, so that the clock cycle must be increased, as shown in Figure 4(a). On the other hand, Figure 4(b) shows that time-borrowing is taking place in the skew-tolerant design since the phase computations extend beyond the nominal quarter-cycle phase boundaries, as indicated by the dashed vertical lines. In this case, the clock cycle time is equal to the propagation delay for logic evaluation alone, since all sources of clocking overhead have been eliminated. The results show that the skew-tolerant domino design is 41% faster than the traditional two-phase clocking design.

4.2. Signed Digit-Serial Multiplier

In this section, a structure for a digit-serial multiplier is proposed for two's complement multiplication, so that it can operate on both positive and negative numbers. Assuming that the multiplicand, A , with W bits, and the multiplier, B , with W bits are two's complement numbers, the product, P becomes

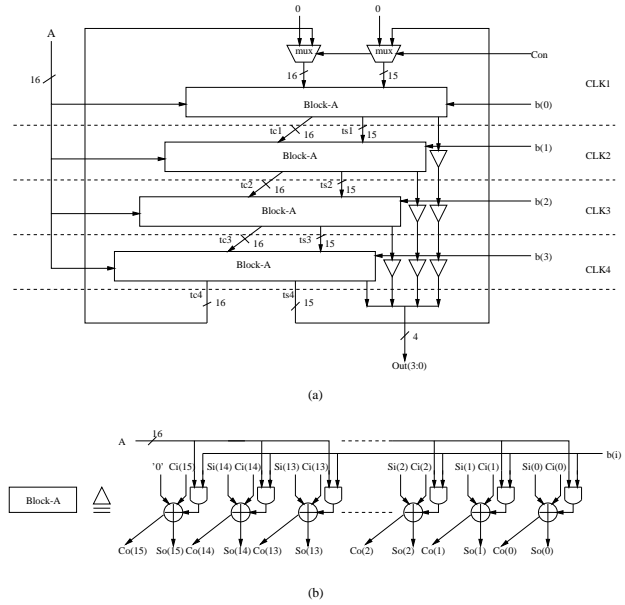


Fig. 3. 16-bit unsigned digit-serial multiplier with a digit size of 4 bits. (a) Top-level design using 4 overlapping clock phases. (b) Implementation of Block-A.

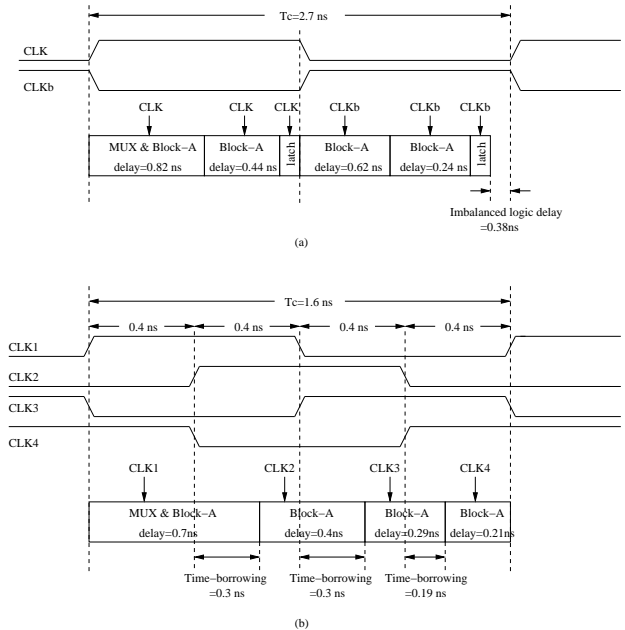


Fig. 4. Simulation results for one full clock cycle. (a) Traditional two-phase clocking scheme. (b) Four-phase overlapping clocking scheme.

$$P = A \cdot B = (-A \cdot b_{W-1}) 2^{W-1} + \sum_{i=0}^{W-2} (A \cdot b_i) 2^i. \quad (1)$$

The algorithm for signed multiplication is based on performing a sign extension of each partial product as well as using the two's complement of A in the last partial product. A signed digit-serial multiplier with a digit-size of 4 bits and 4 overlapping clock phases is illustrated in Figure 5(a). The design consists of four components, called Block-A, Block-B, domino buffer, and MUX. Block-A corresponds to a one-bit multiplication using the partial product generator with sign extension. Block-B corresponds to the last partial product using sign extension and the precomputed two's complement of the multiplicand, $-A$ as shown in Figure 5(b). Note that when the control signal Con is 0, Block-B performs the same function as Block-A. On the other hand, when $Con2 = 1$, the two's complement of the multiplicand, $-A$ is used instead. The multiplicand A and its two's complement are fed into the structure in parallel, while the multiplier, B , is partitioned into 4-bit digits, LSD first. When the last digit of the multiplier (which contains the sign bit) enters, the control signal $Con2$ in Block-B must be high to load the precomputed two's complement, $-A$. The low-order 4 digits of the product, are produced at $out(3 : 0)$, LSD first, in the first 4 clock cycles and the high order 4 digits are obtained by inserting extra zeros into the $b(3 : 0)$ inputs during the second set of 4 clock cycles.

Figures 6(a) and 6(b) show the simulation results for the 16-bit signed digit-serial multiplier with a digit-size of 4 bits, comparing the performance between skew-tolerant domino circuits and traditional domino circuits. As in the case for the unsigned multiplier, the traditional domino circuit suffers from clocking overhead due to imbalanced logic and latch propagation delays, while these are mitigated in the skew-tolerant domino design. In this case, the skew-tolerant domino circuit is 29% faster than the traditional domino implementation.

5. PERFORMANCE EVALUATION

In order to more fully evaluate the performance benefits of our skew-tolerant domino digit-serial multiplier implementations, we compared traditional two-phase domino against N-phase skew-tolerant domino for a range of digit sizes, N. In particular, we designed and simulated with a word size of 16 bits and a digit size of $N = 2, 4$ and 8 bits (using 2, 4, and 8 overlapping clock phases, respectively). This type of analysis can provide a designer with the necessary information to find the best compromise between area and performance for a given application under consideration. As in the previous section, all simulations are performed using a 0.25 micron TSMC CMOS technology with a supply

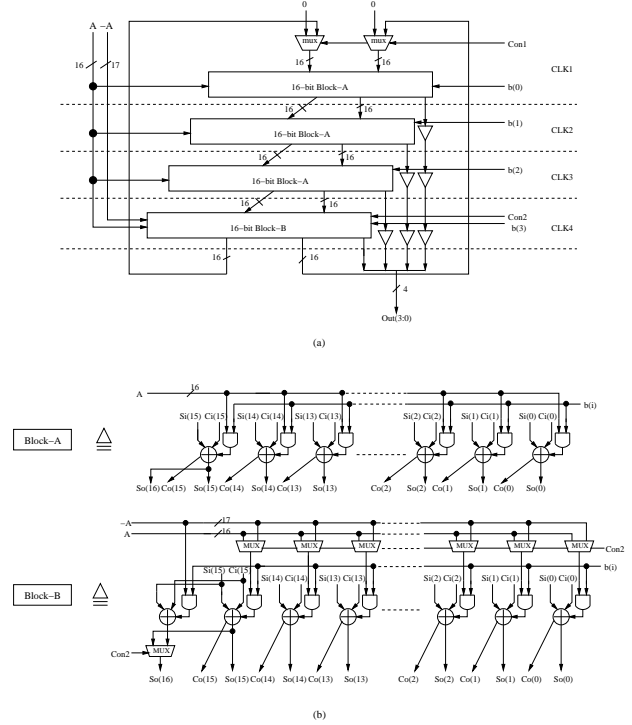


Fig. 5. 16-bit signed digit-serial multiplier with a digit size of 4 bits. (a) Top-level design using 4 overlapping clock phases. (b) Implementations of Block-A and Block-B.

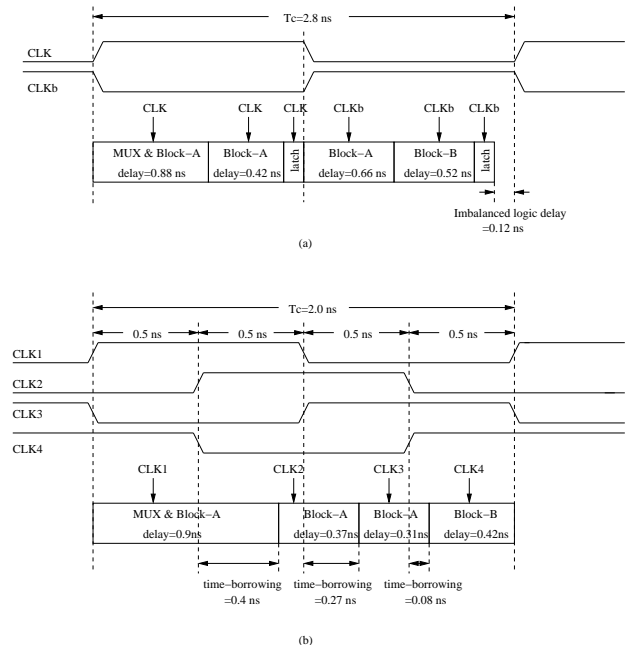


Fig. 6. Simulation results for one full clock cycle. (a) Traditional two-phase clocking scheme. (b) Four-phase overlapping clocking scheme.

voltage of 2.5V, under nominal process and environmental conditions. Figures 7(a) and 7(b) show the clock cycle time and throughput (measured in bits/ns) corresponding to the digit sizes of $N = 2, 4$ and 8 bits.

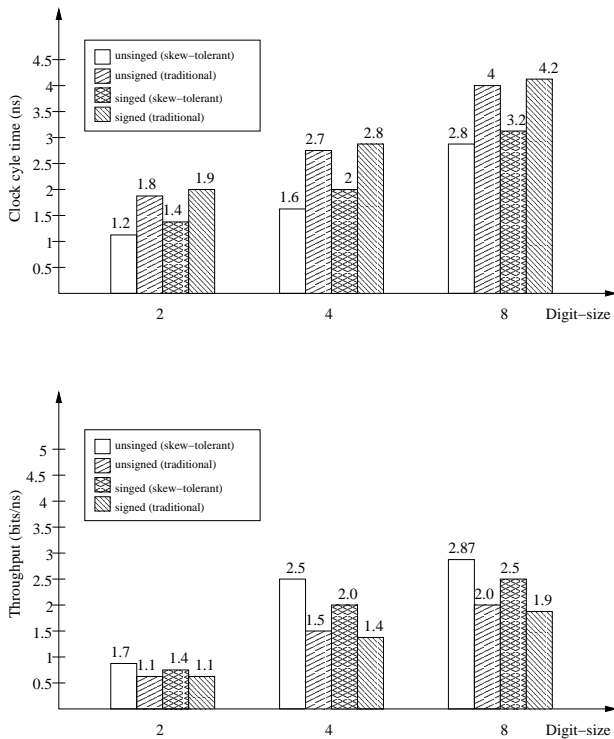


Fig. 7. Performance comparisons of various unsigned and signed digit-serial multipliers implemented with skew-tolerant domino and traditional two-phase domino. (a) Clock cycle times with $N = 2, 4$, and 8. (b) Throughput with $N = 2, 4$, and 8.

In each sub-case, the first and second bars represent the results for skew-tolerant domino and traditional two-phase domino circuits, respectively, for the unsigned multiplier designs. The third and fourth bars represent the results for skew-tolerant domino and traditional two-phase domino, respectively, for the signed multiplier designs. The simulation results show that skew-tolerant domino circuits are faster than traditional domino circuits in all cases, with the largest percentage improvement being achieved in the case where the digit size $N = 4$.

6. CONCLUSIONS

We have proposed a novel design methodology for unsigned and signed digit-serial multipliers based on a unique connection between digit-serial computation and skew-tolerant domino circuit techniques. A digit-serial structure with a digit size of N bits is mapped in a natural fashion onto a

skew-tolerant domino clocking scheme with N overlapping clock phases. In this way, one bit is utilized during each of N phases, so that an N -bit digit is processed in each full clock cycle. This leads to simple scheduling and straightforward implementations of digit-serial systems. We have simulated unsigned and signed multipliers using skew-tolerant domino circuits and traditional domino circuits and compared their relative performances. The results confirm that the skew-tolerant domino circuits improve the throughput of digit-serial multipliers by up to 41% over the traditional two-phase clocking design.

7. REFERENCES

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